AG1 Block Diagram

Project code: 91.4A901.001
PCB P/N : 55.4A903.XXX
REVISION : 05225-1
(Hannstar, GCE)

PCB STACKUP

TOP
VCC
S
S
GND
BUTTOM

CLK GEN.
ICS954305D
(IDT CV155) 3

Mobile CPU
Yonah 478
Celeron M 4, 5

G792 19

HOST BUS 400/533/667MHz

DDR2 533/667 MHz 11,12
533/667MHz

DDR2 533/667 MHz 11,12
533/667MHz

Calistoga 6,7,8,9,10

TVO 14

LVDS 14"WSXGA+ LCD 13

RGB CRT CRT 14

DMI I/F 100MHz

ICH7-M 15,16,17,18

Line In 29
MIC In 29
Codec ALC883 28
AZALIA

Line Out (SPDIF) 29
OP AMP G1421B 29

INT.SPKR 29

RJ11
MODEM MDC Card 21

PCI Express
New card 30
PWR SW TPS2231 30

SATA
HDD 20

PATA
CDROM 18

USB 3 PORT 21
MINI USB Blue-tooth 21

PCI BUS
TI PCI 7412
CARDBUS 1394 CardReader 24,25

PCMCIA I/F
PWR SW TSP2220A 27
PCMCIA SLOT Support TypeII 27

1394 CONN 26

MS/MS Pro/xD/ MMC/SD/SDIO 6 in 1 26

Mini-PCI TV Tuner 30

LAN 10/100 BCM4401-E 22
TXFM 23
RJ45 23

PCIEx1
Mini Card*2 802.11A/B/G 26

Giga LAN 22 BCM5798

SPI I/F
SPI Flash

LPC BUS
SIO NS 87392 32
FIR 32

KBC HD64F2111BVC 31
Touch Pad 33
INT. KB 33

LPC DEBUG CONN. 34

SYSTEM DC/DC
TPS51120 41

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5

SYSTEM DC/DC
MAX8743EE 42

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

TPS51100 44

1D8V_S3	DDR_VREF

APL5332KAC 44

3D3V_S5	2D5V_S0

APL5912-U 44

3D3V_S5	1D5V_S0

MAXIM CHARGER
MAX8725+Max1773 43

INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A UP+5V 5V 100mA

CPU DC/DC
ISL6262 39,40

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 48A

<Variant Name>

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Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	AG1	-1

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ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS, SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

954305D 27Mhz/LCDCLK Spread and Frequency Selection Table

page 3

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	-0.50 Down
0	0	0	1	-1.00 Down
0	0	1	0	-1.50 Down
0	0	1	1	-2.00 Down
0	1	0	0	-0.75 Down
0	1	0	1	-1.25 Down
0	1	1	0	-1.75 Down
0	1	1	1	-2.25 Down
1	0	0	0	+-0.25 Center
1	0	0	1	+-0.5 Center
1	0	1	0	+-0.75 Center
1	0	1	1	+-1.0 Center
1	1	0	0	+-0.25 Center
1	1	0	1	+-0.5 Center
1	1	1	0	+-0.75 Center
1	1	1	1	+-1.0 Center

PCI Routing

page 16

	IDSEL	INT -> PIRQ	REQ/GNT
7412	22	A->G, B->B, C->F, D->G	0
MiniPCI	21	A/C -> E B/D -> E	1
LAN	23	A -> H	2
1410	25	A->G, B->B,	0

Calistoga Strapping Signals and Configuration

EDS 17050 0.71

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

History

6/6 drawing SA
7/11 Rename for placement

<Variant Name>

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Title: Reference

Size: A3 | Document Number: AG1 | Rev: -1

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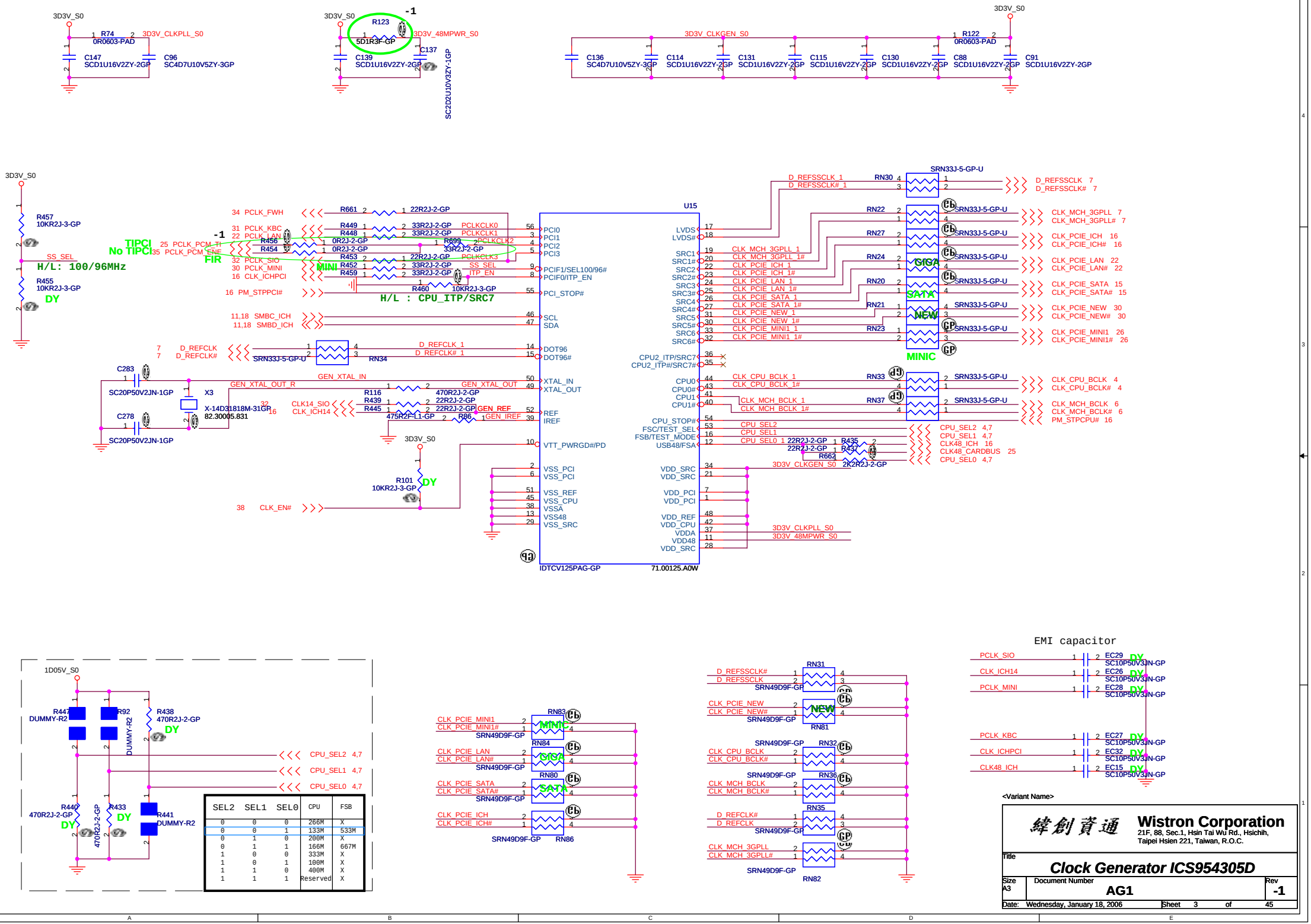
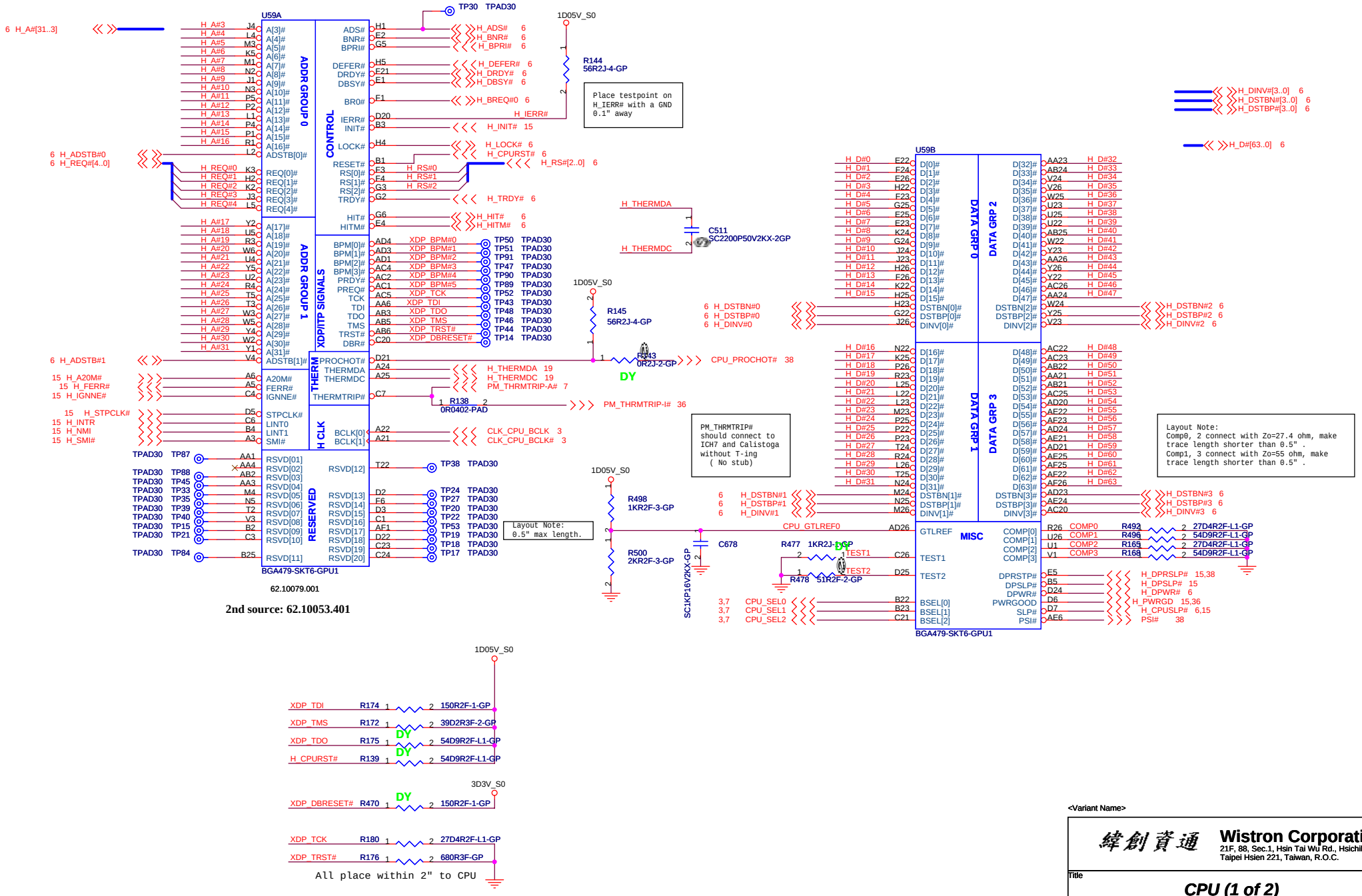
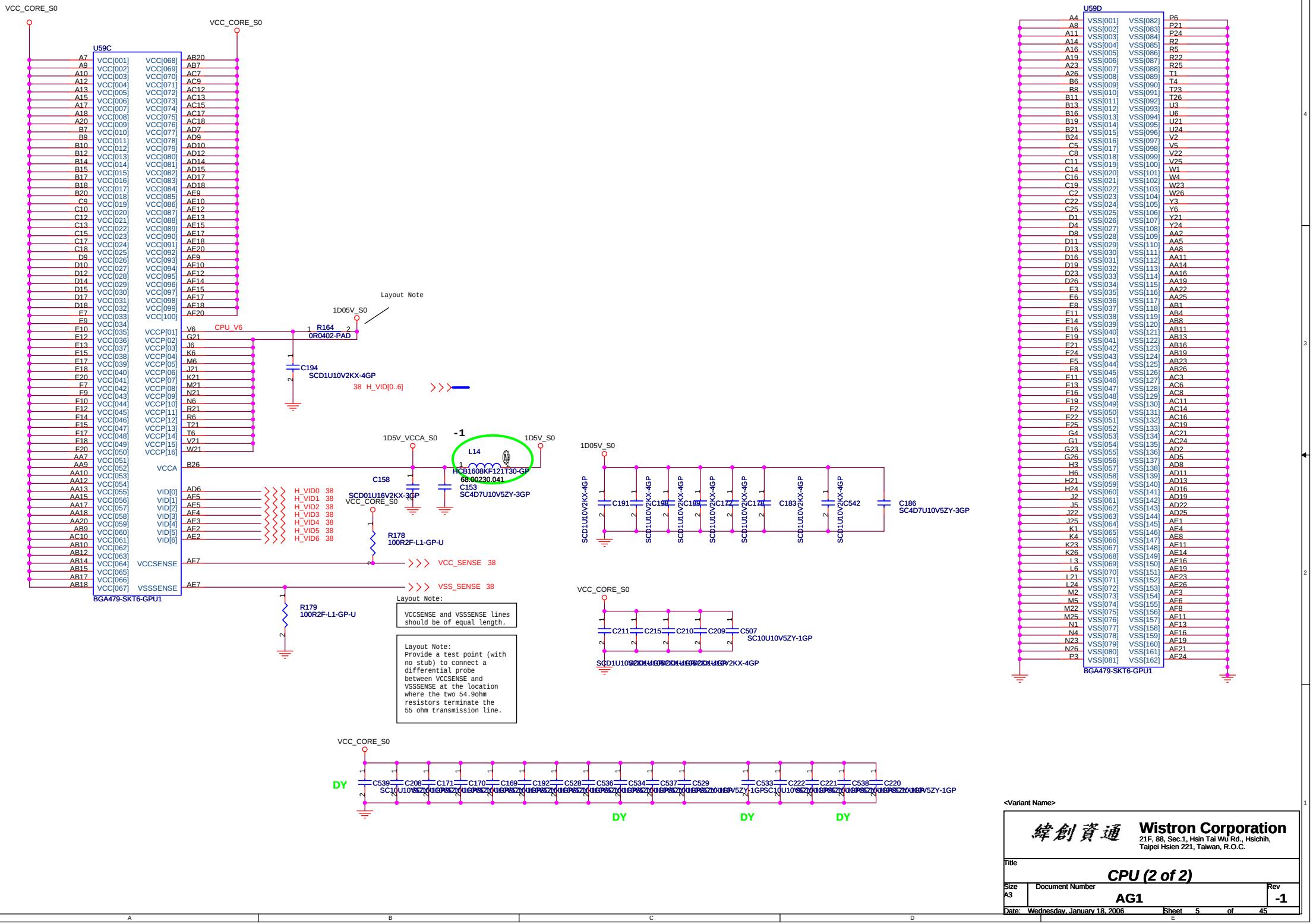

3D3V_S0
R74 0R0603-PAD 3D3V_CLKPLL_S0
C147 SCD1U16V2ZY-2GP
C96 SC4D7U10V5ZY-3GP
R123 5D1R3F-GP -1 3D3V_48MPWR_S0
C139 SCD1U16V2ZY-2GP
C137 SC2D2U10V3ZY-1GP
3D3V_CLKGEN_S0
C136 SC4D7U10V5ZY-3GP
C114 SCD1U16V2ZY-2GP
C131 SCD1U16V2ZY-2GP
C115 SCD1U16V2ZY-2GP
C130 SCD1U16V2ZY-2GP
R122 0R0603-PAD
C88 SCD1U16V2ZY-2GP
C91 SCD1U16V2ZY-2GP
R457 10KR2J-3-GP
SS_SEL
H/L: 100/96MHz
R455 10KR2J-3-GP
DY
TIPCI
No TIPCI
FIR
MINI
-1
34 PCLK_FWH
31 PCLK_KBC
22 PCLK_LAN
25 PCLK_PCM_TI
35 PCLK_PCM_ENE
32 PCLK_SIO
30 PCLK_MINI
16 CLK_ICHPCI
16 PM_STPPCI#
R661 22R2J-2-GP
R449 33R2J-2-GP PCLKCLK0
R448 33R2J-2-GP PCLKCLK1
R456 0R2J-2-GP
R454 0R2J-2-GP
R699 33R2J-2-GP PCLKCLK2
R453 22R2J-2-GP PCLKCLK3
R452 33R2J-2-GP SS_SEL
R459 33R2J-2-GP ITP_EN
R460 10KR2J-3-GP
H/L : CPU_ITP/SRC7
11,18 SMBC_ICH
11,18 SMBD_ICH
7 D_REFCLK
7 D_REFCLK#
SRN33J-5-GP-U RN34
D_REFCLK_1
D_REFCLK#_1
C283 SC20P50V2JN-1GP
C278 SC20P50V2JN-1GP
X3 X-14D31818M-31GP 82.30005.831
GEN_XTAL_OUT_R
GEN_XTAL_IN
GEN_XTAL_OUT
R116 470R2J-2-GP
R439 22R2J-2-GP
R445 22R2J-2-GP
475R2F-L1-GP R86
CLK14_SIO
CLK_ICH14
GEN_REF
GEN_IREF
R101 10KR2J-3-GP DY
38 CLK_EN#
U15
PCI0 PCI1 PCI2 PCI3 PCIF1/SEL100/96# PCIF0/ITP_EN PCI_STOP# SCL SDA DOT96 DOT96# XTAL_IN XTAL_OUT REF IREF VTT_PWRGD#/PD
VSS_PCI VSS_PCI VSS_REF VSS_CPU VSSA VSS48 VSS_SRC
LVDS LVDS# SRC1 SRC1# SRC2 SRC2# SRC3 SRC3# SRC4 SRC4# SRC5 SRC5# SRC6 SRC6#
CPU2_ITP/SRC7 CPU2_ITP#/SRC7#
CPU0 CPU0# CPU1 CPU1#
CPU_STOP# FSC/TEST_SEL FSB/TEST_MODE USB48/FSA
VDD_SRC VDD_SRC VDD_PCI VDD_PCI VDD_REF VDD_CPU VDDA VDD48 VDD_SRC
IDTCV125PAG-GP 71.00125.A0W
D_REFSSCLK_1 D_REFSSCLK# 1 RN30 SRN33J-5-GP-U
D_REFSSCLK 7 D_REFSSCLK# 7
RN22 CLK_MCH_3GPLL_1 CLK_MCH_3GPLL_1# CLK_MCH_3GPLL 7 CLK_MCH_3GPLL# 7
RN27 CLK_PCIE_ICH_1 CLK_PCIE_ICH_1# CLK_PCIE_ICH 16 CLK_PCIE_ICH# 16
RN24 CLK_PCIE_LAN_1 CLK_PCIE_LAN_1# CLK_PCIE_LAN 22 CLK_PCIE_LAN# 22
RN20 CLK_PCIE_SATA_1 CLK_PCIE_SATA_1# CLK_PCIE_SATA 15 CLK_PCIE_SATA# 15
RN21 CLK_PCIE_NEW_1 CLK_PCIE_NEW_1# CLK_PCIE_NEW 30 CLK_PCIE_NEW# 30
RN23 CLK_PCIE_MINI1_1 CLK_PCIE_MINI1_1# CLK_PCIE_MINI1 26 CLK_PCIE_MINI1# 26
SRN33J-5-GP-U
GIGA SATA NEW GP MINIC
RN33 CLK_CPU_BCLK_1 CLK_CPU_BCLK_1# CLK_CPU_BCLK 4 CLK_CPU_BCLK# 4
RN37 CLK_MCH_BCLK_1 CLK_MCH_BCLK_1# CLK_MCH_BCLK 6 CLK_MCH_BCLK# 6 PM_STPCPU# 16
CPU_SEL2 CPU_SEL1 CPU_SEL0 1 22R2J-2-GP R435 22R2J-2-GP R437 R662 2K2R2J-2-GP 3D3V_CLKGEN_S0
CPU_SEL2 4,7
CPU_SEL1 4,7
CLK48_ICH 16
CLK48_CARDBUS 25
CPU_SEL0 4,7
3D3V_CLKPLL_S0
3D3V_48MPWR_S0
1D05V_S0
R447 DUMMY-R2
R92 DUMMY-R2
R438 470R2J-2-GP DY
CPU_SEL2 4,7
CPU_SEL1 4,7
CPU_SEL0 4,7
R440 470R2J-2-GP DY
R433 DY
R441 DUMMY-R2
SEL2 SEL1 SEL0 CPU FSB
0 0 0 266M X
0 0 1 133M 533M
0 1 0 200M X
0 1 1 166M 667M
1 0 0 333M X
1 0 1 100M X
1 1 0 400M X
1 1 1 Reserved X
CLK_PCIE_MINI1 CLK_PCIE_MINI1# SRN49D9F-GP RN83 MINIC
CLK_PCIE_LAN CLK_PCIE_LAN# SRN49D9F-GP RN84 GIGA
CLK_PCIE_SATA CLK_PCIE_SATA# SRN49D9F-GP RN80 SATA
CLK_PCIE_ICH CLK_PCIE_ICH# SRN49D9F-GP RN86
D_REFSSCLK# D_REFSSCLK SRN49D9F-GP RN31
CLK_PCIE_NEW CLK_PCIE_NEW# SRN49D9F-GP RN81 NEW GP
CLK_CPU_BCLK CLK_CPU_BCLK# SRN49D9F-GP RN32
CLK_MCH_BCLK CLK_MCH_BCLK# SRN49D9F-GP RN36
D_REFCLK# D_REFCLK SRN49D9F-GP RN35
CLK_MCH_3GPLL CLK_MCH_3GPLL# SRN49D9F-GP RN82
EMI capacitor
PCLK_SIO EC29 SC10P50V3JN-GP DY
CLK_ICH14 EC26 SC10P50V3JN-GP DY
PCLK_MINI EC28 SC10P50V3JN-GP DY
PCLK_KBC EC27 SC10P50V3JN-GP DY
CLK_ICHPCI EC32 SC10P50V3JN-GP DY
CLK48_ICH EC15 SC10P50V3JN-GP DY
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator ICS954305D
Size A3
Document Number AG1
Rev -1
Date: Wednesday, January 18, 2006
Sheet 3 of 45



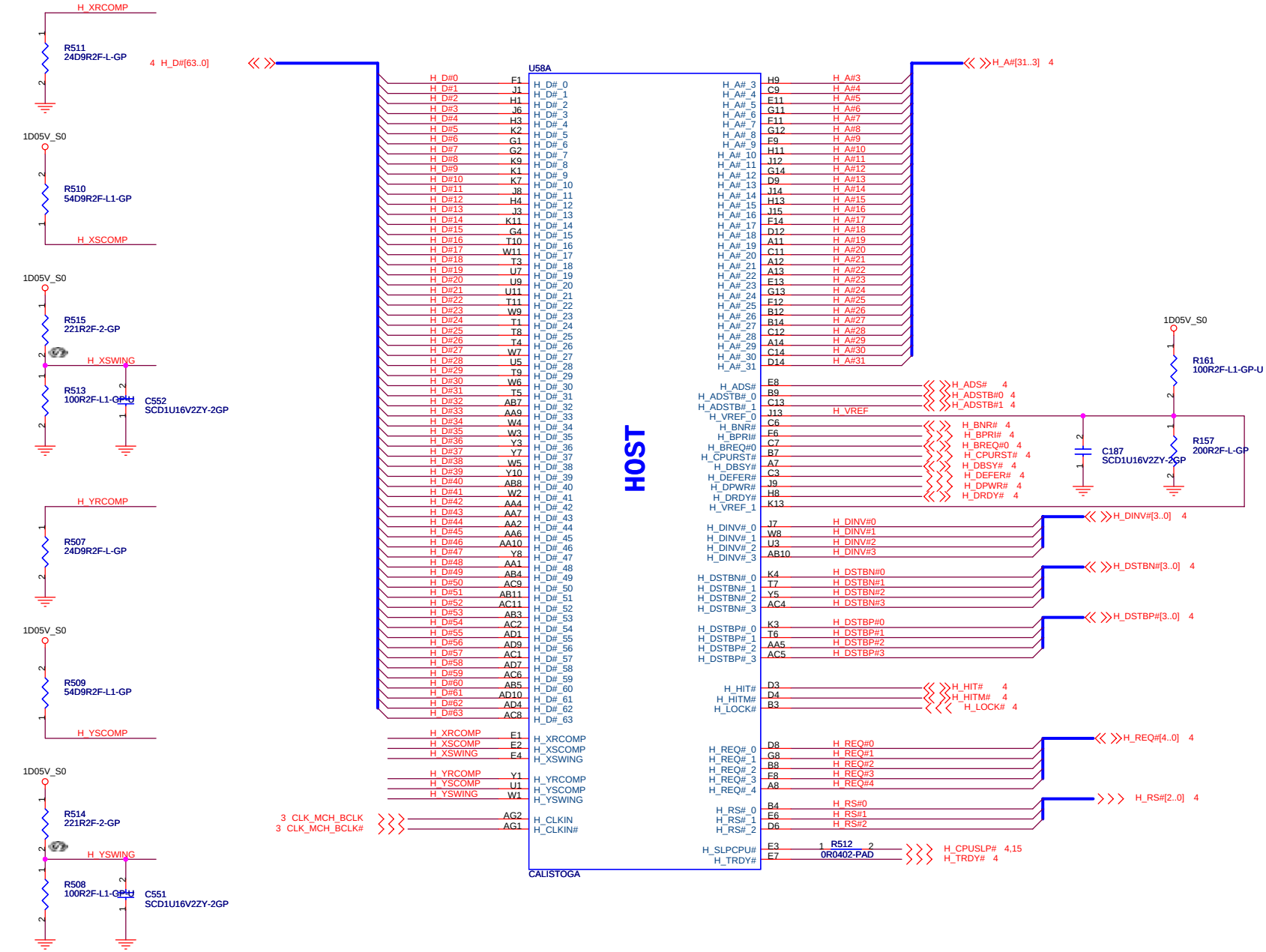
<variant_name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU (1 of 2)***	
Size A3	Document Number **AG1**	Rev **-1**
Date: Wednesday, January 18, 2006	Sheet 4 of 45	



<Variant Name>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU (2 of 2)
Size A3	Document Number AG1
Rev	-1
Date: Wednesday, January 18, 2006	Sheet 5 of 45



Place them near to the chip (< 0.5")

<Variant Name>

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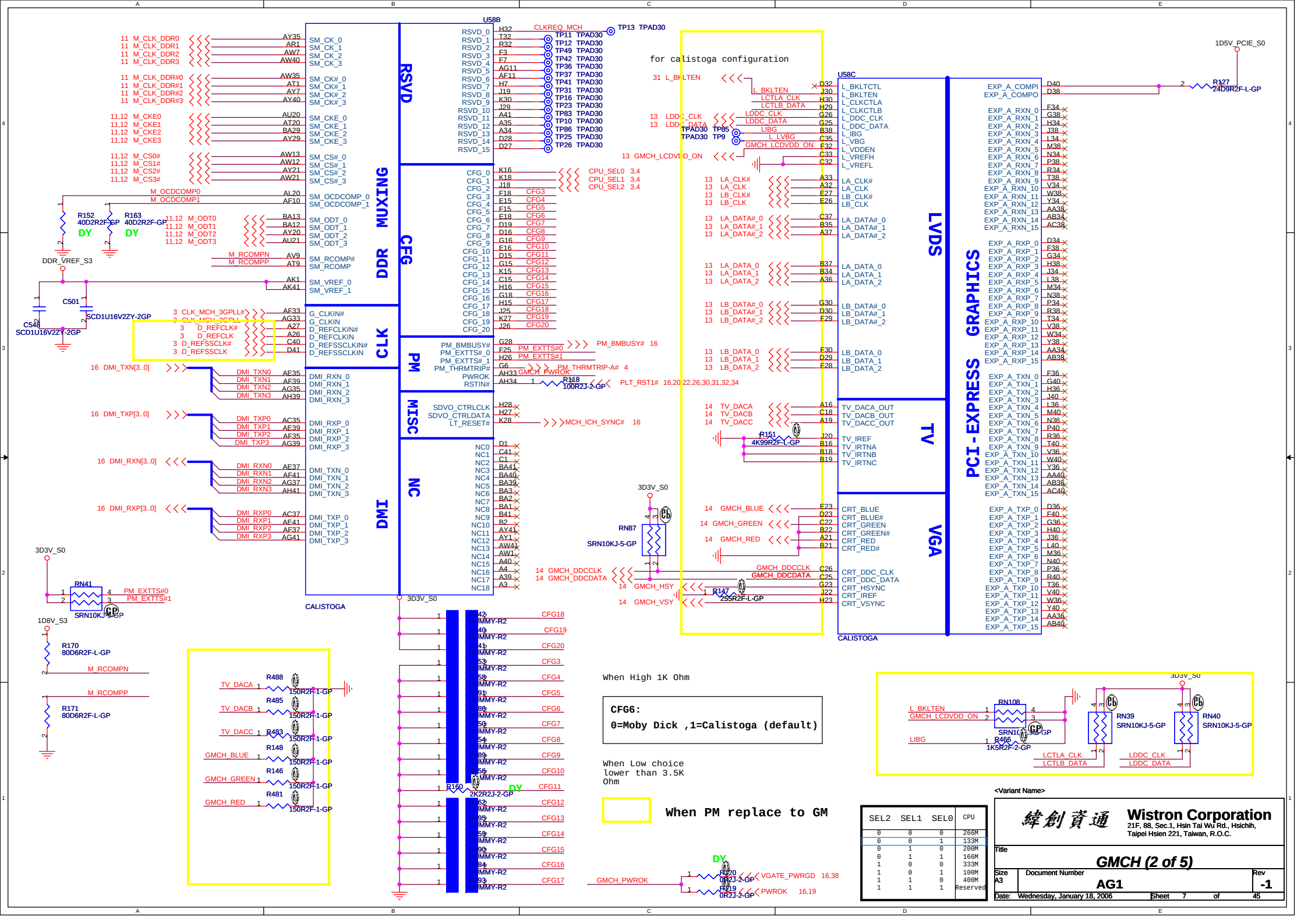
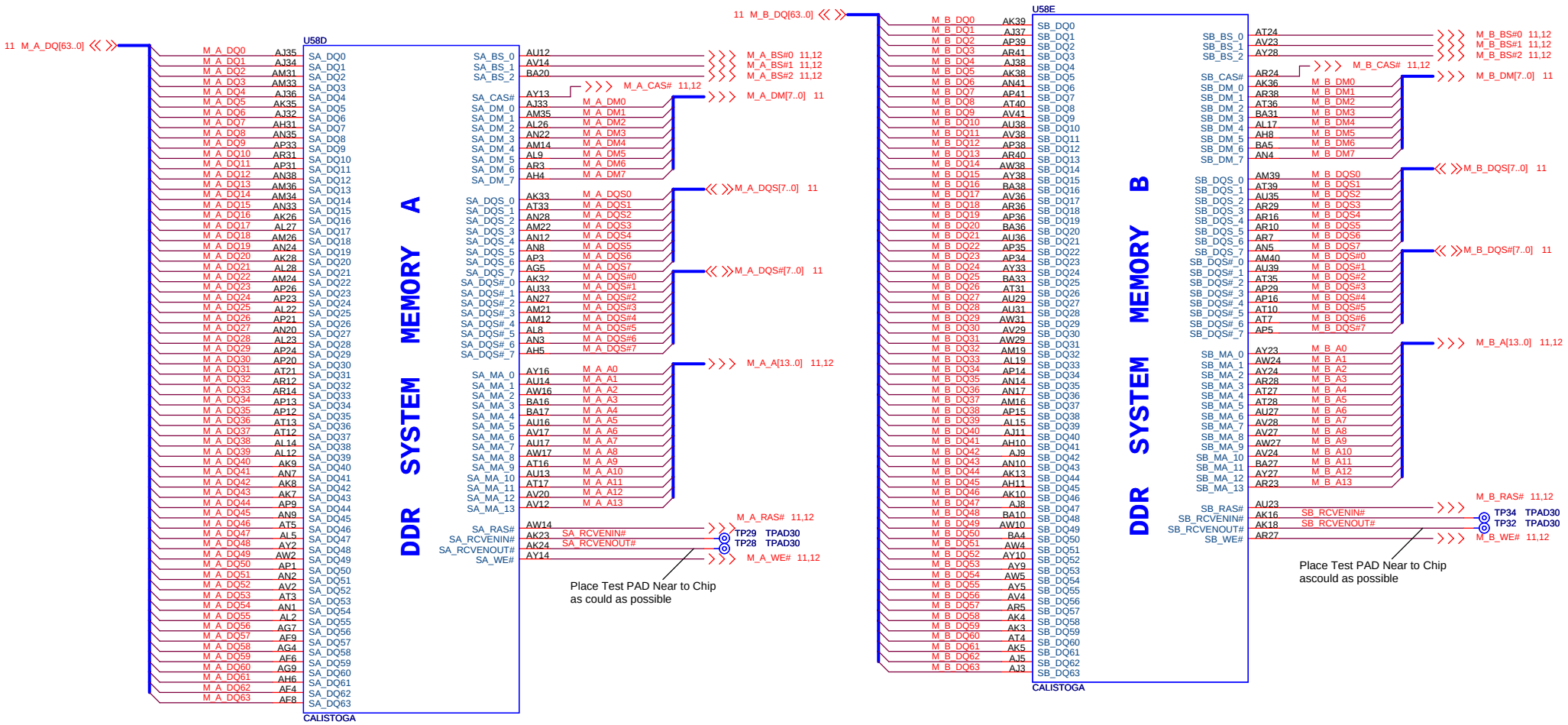
Title: GMCH (1 of 5)

Size: A3 | Document Number: AG1 | Rev: -1

Date: Wednesday, January 18, 2006 | Sheet 6 of 45


U58B
RSVD
CFG
PM
MISC
NC
DDR MUXING
CLK
DMI
CALISTOGA
for calistoga configuration
U58C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
CALISTOGA
When High 1K Ohm
CFG6:
0=Moby Dick ,1=Calistoga (default)
When Low choice lower than 3.5K Ohm
When PM replace to GM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
GMCH (2 of 5)
AG1
-1
Wednesday, January 18, 2006
Sheet 7 of 45



<Variant Name>

緯創資通 **Wistron Corporation**
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Title: ***GMCH (3 of 5)***

Size	Document Number	Rev
A3	AG1	-1

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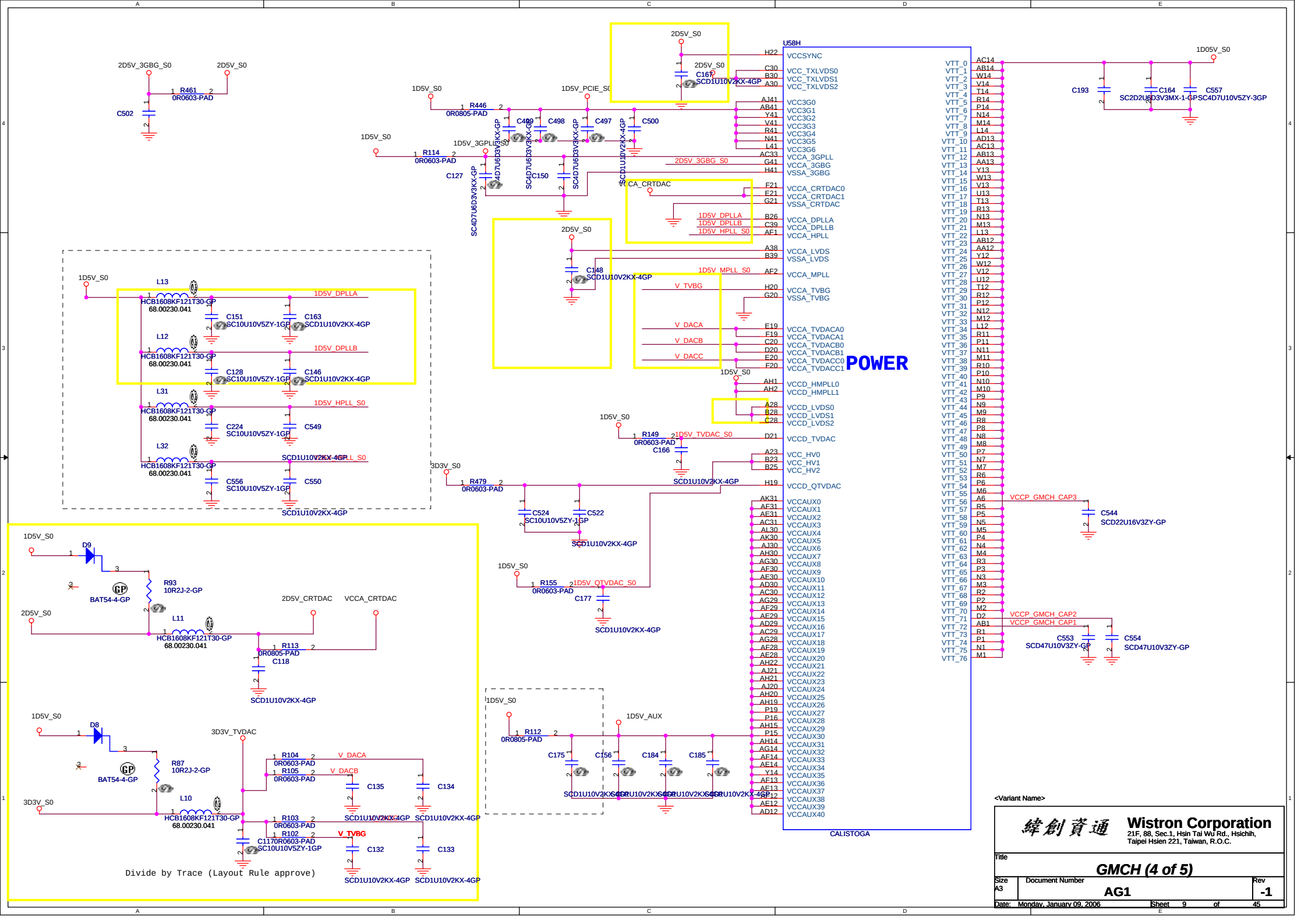
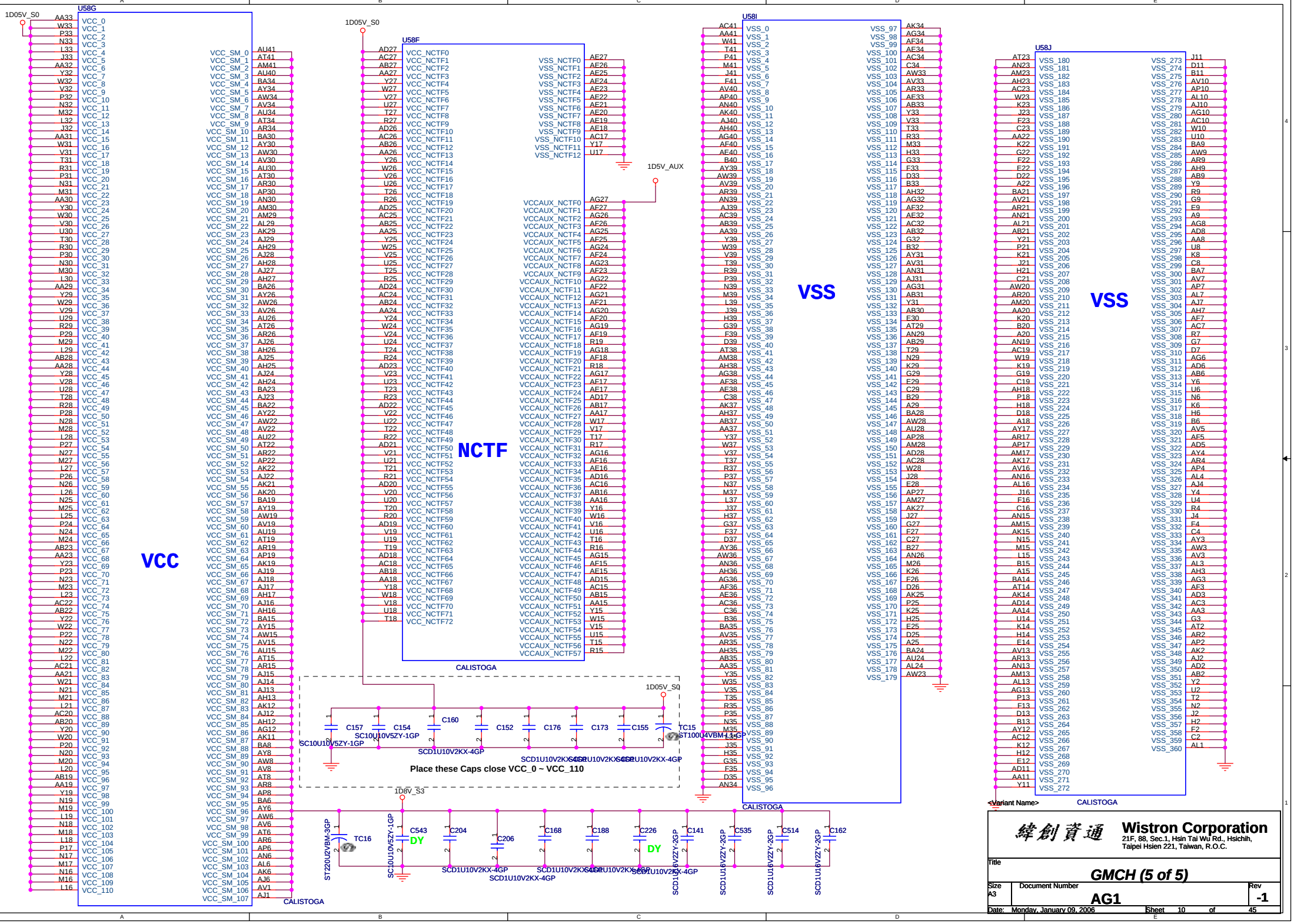

U58H
CALISTOGA
POWER
2D5V_S0
1D5V_S0
3D3V_S0
2D5V_3GBG_S0
1D5V_PCIE_S0
1D5V_3GPLL_S0
VCCA_CRTDAC
1D5V_DPLLA
1D5V_DPLLB
1D5V_HPLL_S0
1D5V_MPLL_S0
V_TVBG
V_DACA
V_DACB
V_DACC
1D5V_TVDAC_S0
1D5V_QTVDAC_S0
1D5V_AUX
3D3V_TVDAC
VCCP_GMCH_CAP3
VCCP_GMCH_CAP2
VCCP_GMCH_CAP1
Divide by Trace (Layout Rule approve)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
GMCH (4 of 5)
AG1
-1
Monday, January 09, 2006
9
45



Wistron Corporation	緯創資通
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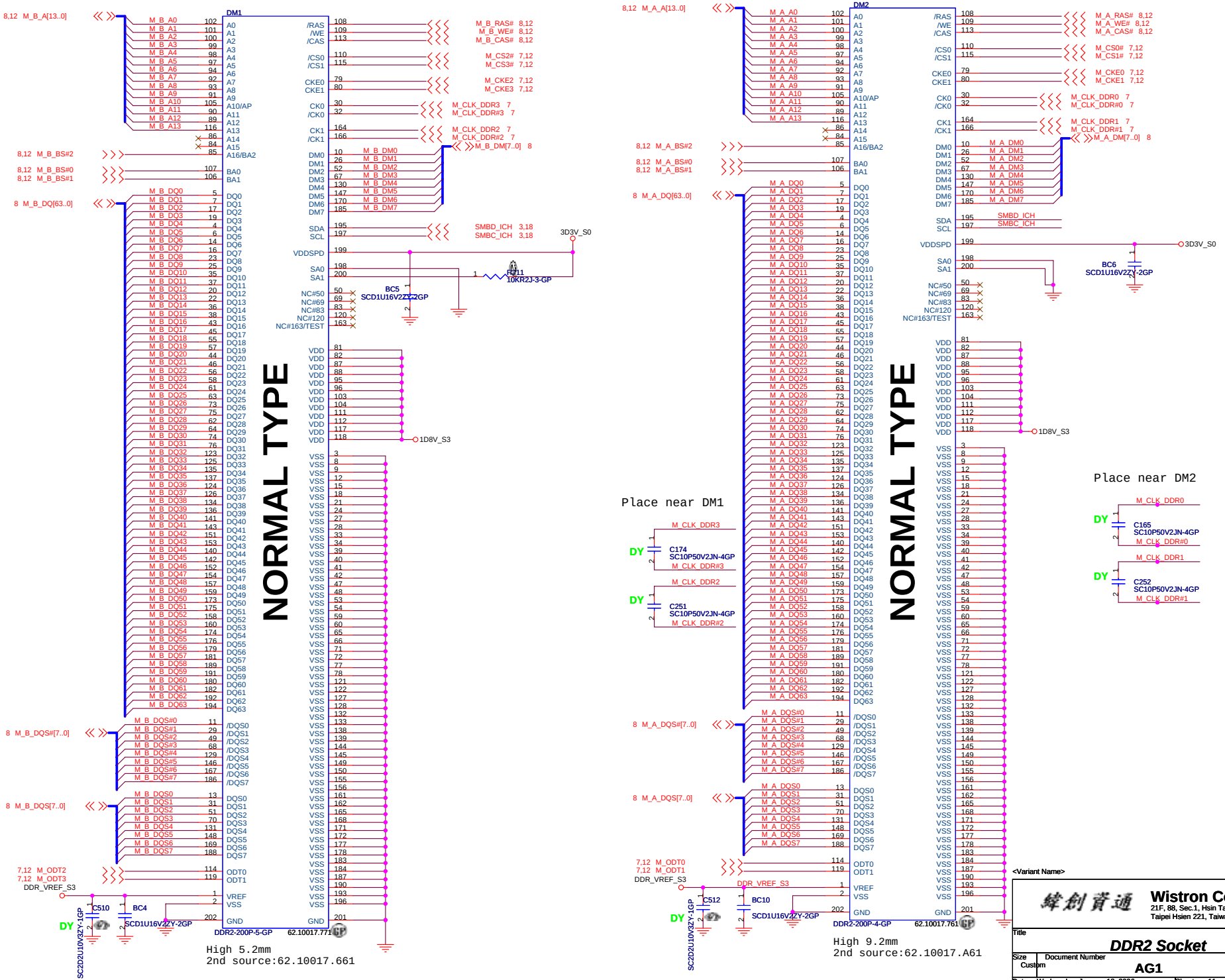
Title	GMCH (5 of 5)
Size A3	Document Number AG1
Rev	-1
Date: Monday, January 09, 2006	Sheet 10 of 45


DM1
NORMAL TYPE
8,12 M_B_A[13..0]
8,12 M_B_BS#2
8,12 M_B_BS#0
8,12 M_B_BS#1
8 M_B_DQ[63..0]
8 M_B_DQS#[7..0]
8 M_B_DQS[7..0]
7,12 M_ODT2
7,12 M_ODT3
DDR_VREF_S3
M_B_RAS# 8,12
M_B_WE# 8,12
M_B_CAS# 8,12
M_CS2# 7,12
M_CS3# 7,12
M_CKE2 7,12
M_CKE3 7,12
M_CLK_DDR3 7
M_CLK_DDR#3 7
M_CLK_DDR2 7
M_CLK_DDR#2 7
M_B_DM[7..0] 8
SMBD_ICH 3,18
SMBC_ICH 3,18
3D3V_S0
1D8V_S3
R211
10KR2J-3-GP
BC5
SCD1U16V2ZY-2GP
C510
BC4
SCD1U16V2ZY-2GP
SC22D2U10V3ZY-1GP
DDR2-200P-5-GP
62.10017.771
High 5.2mm
2nd source:62.10017.661
DM2
NORMAL TYPE
8,12 M_A_A[13..0]
8,12 M_A_BS#2
8,12 M_A_BS#0
8,12 M_A_BS#1
8 M_A_DQ[63..0]
8 M_A_DQS#[7..0]
8 M_A_DQS[7..0]
7,12 M_ODT0
7,12 M_ODT1
DDR_VREF_S3
M_A_RAS# 8,12
M_A_WE# 8,12
M_A_CAS# 8,12
M_CS0# 7,12
M_CS1# 7,12
M_CKE0 7,12
M_CKE1 7,12
M_CLK_DDR0 7
M_CLK_DDR#0 7
M_CLK_DDR1 7
M_CLK_DDR#1 7
M_A_DM[7..0] 8
SMBD_ICH
SMBC_ICH
3D3V_S0
1D8V_S3
BC6
SCD1U16V2ZY-2GP
Place near DM1
M_CLK_DDR3
C174
SC10P50V2JN-4GP
M_CLK_DDR#3
M_CLK_DDR2
C251
SC10P50V2JN-4GP
M_CLK_DDR#2
Place near DM2
M_CLK_DDR0
C165
SC10P50V2JN-4GP
M_CLK_DDR#0
M_CLK_DDR1
C252
SC10P50V2JN-4GP
M_CLK_DDR#1
C512
BC10
SCD1U16V2ZY-2GP
SC22D2U10V3ZY-1GP
DDR2-200P-4-GP
62.10017.761
High 9.2mm
2nd source:62.10017.A61
<Variant Name>
蜂創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR2 Socket
Size
Custom
Document Number
AG1
Rev
-1
Date: Wednesday, January 18, 2006
Sheet 11 of 45

PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

RN44 SRN56J-2-GP
- 1 M_CKE2 7,11
- 2 M_B_BS#2 8,11
- 3 M_B_A12
- 4 M_B_A9

M_A_A[13..0] 8,11

M_B_A[13..0] 8,11

R186 56R2J-4-GP M_ODT1 7,11
R187 56R2J-4-GP M_ODT3 7,11
R192 56R2J-4-GP M_A_A9
R184 56R2J-4-GP M_B_A8

RN47 SRN56J-2-GP
- 1 M_B_A5
- 2 M_B_A3
- 3 M_B_A1
- 4 M_B_A10

RN53 SRN56J-2-GP
- 1 M_B_A13
- 2 M_ODT2 7,11
- 3 M_CS2# 7,11
- 4 M_B_RAS# 8,11

RN49 SRN56J-2-GP
- 1 M_B_BS#1 8,11
- 2 M_B_A0
- 3 M_B_A2
- 4 M_B_A4

RN45 SRN56J-2-GP
- 1 M_B_A6
- 2 M_B_A7
- 3 M_B_A11
- 4 M_CKE3 7,11

RN52 SRN56J-2-GP
- 1 M_B_BS#0 8,11
- 2 M_B_WE# 8,11
- 3 M_CS3# 7,11
- 4 M_B_CAS# 8,11

RN54 SRN56J-2-GP
- 1 M_A_A13
- 2 M_ODT0 7,11
- 3 M_CS0# 7,11
- 4 M_A_RAS# 8,11

RN50 SRN56J-2-GP
- 1 M_A_BS#1 8,11
- 2 M_A_A0
- 3 M_A_A2
- 4 M_A_A4

RN51 SRN56J-2-GP
- 1 M_A_BS#0 8,11
- 2 M_A_WE# 8,11
- 3 M_A_CAS# 8,11
- 4 M_CS1# 7,11

RN43 SRN56J-2-GP
- 1 M_CKE0 7,11
- 2 M_A_BS#2 8,11
- 3 M_A_A12
- 4 M_A_A8

RN46 SRN56J-2-GP
- 1 M_A_A6
- 2 M_A_A7
- 3 M_A_A11
- 4 M_CKE1 7,11

RN48 SRN56J-2-GP
- 1 M_A_A5
- 2 M_A_A3
- 3 M_A_A1
- 4 M_A_A10

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

C229 C231 C219 C246 C236 C214 C232 C240 C237 C245 C223 SCD1U16V2ZY-2GP DY DY
C216 C227 C233 C228 C239 C235 C244 C230 C241 C218 C213 SCD1U16V2ZY-2GP DY DY

1D8V_S3

Place these Caps near DM1

C205 C200 C197 C201 C559 SC2D2U6D3V3MX-1-GP
C558 C212 C555 C546 SCD1U16V2ZY-2GP DY DY DY

1D8V_S3

Place these Caps near DM2

C565 C203 C225 C217 C560 SC2D2U6D3V3MX-1-GP
C207 C196 C247 C547 SCD1U16V2ZY-2GP DY DY DY

<Variant Name>

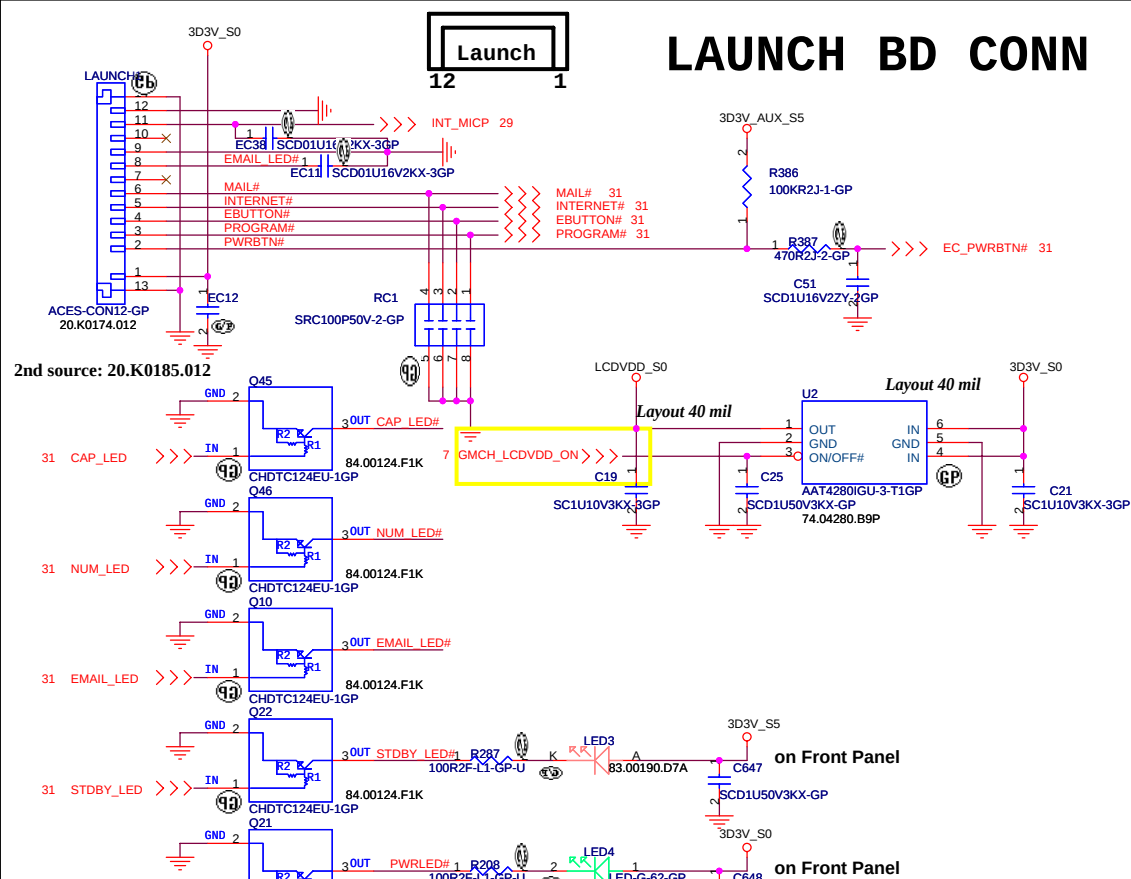
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR2 Termination Resistor***

Size	Document Number	Rev
A3	AG1	-1

Date: Wednesday, January 18, 2006 Sheet 12 of 45

LAUNCH BD CONN

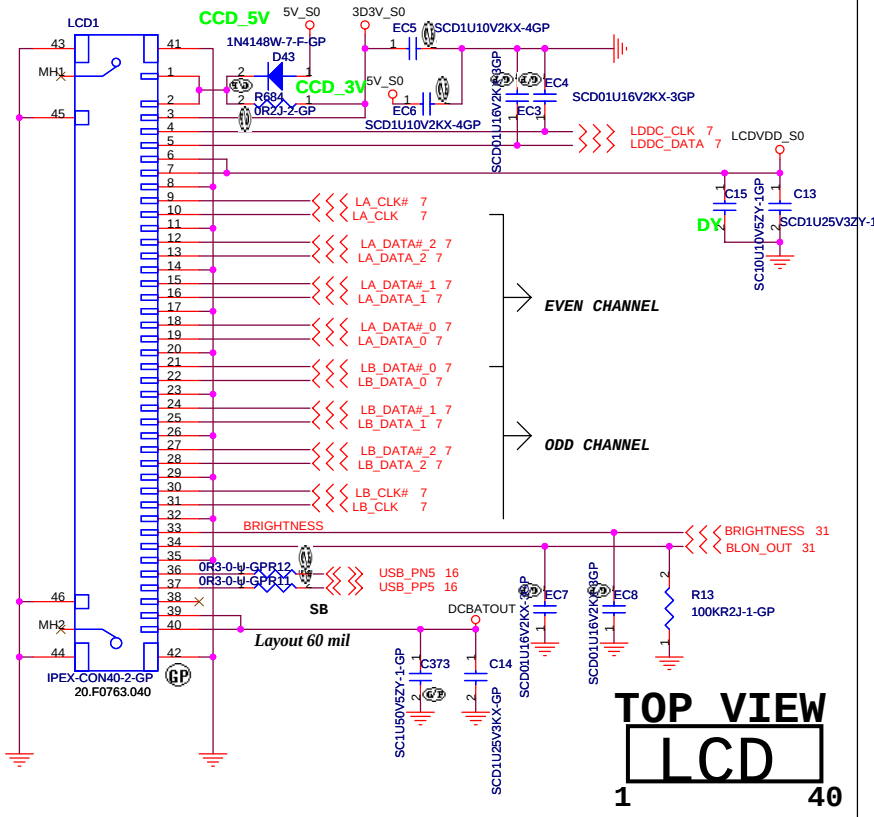


CCD Pin	
Pin	Symbol
1	5V
2	USB-
3	USB+
4	GND
5	GND

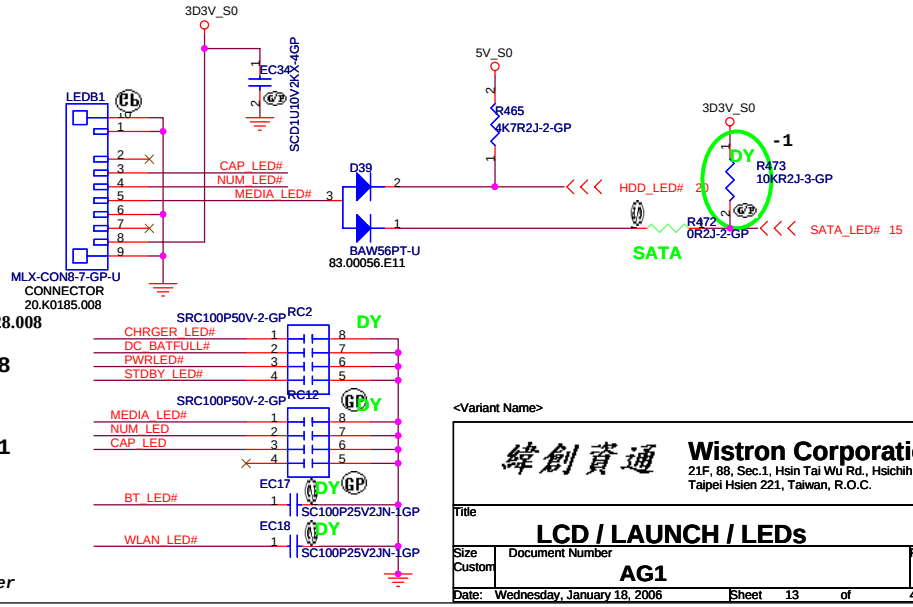
Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

Launch BD	
Pin	Symbol
1	3V_S0
2	PWRBTN#
3	PROGRAM#
4	EBUTTON#
5	INTERNET#
6	MAIL#
7	NC
8	MAIL_LED#
9	PWR_B_LED#
10	NC
11	INT_MICP
12	INT_MICN

LCD/INVERTER/CCD CONN



LED BD CONN



Charger:
OFF : Battery or DC only
Orange : Charging
Orange Blink : Battery low

Power:
Green : S0
Orange : S3
Orange Blinking : Enter S4

Front panel

LED	V	V	V	V
Button	V	V		
	BlutTooth	Wireless	Charger	Power2

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD / LAUNCH / LEDs

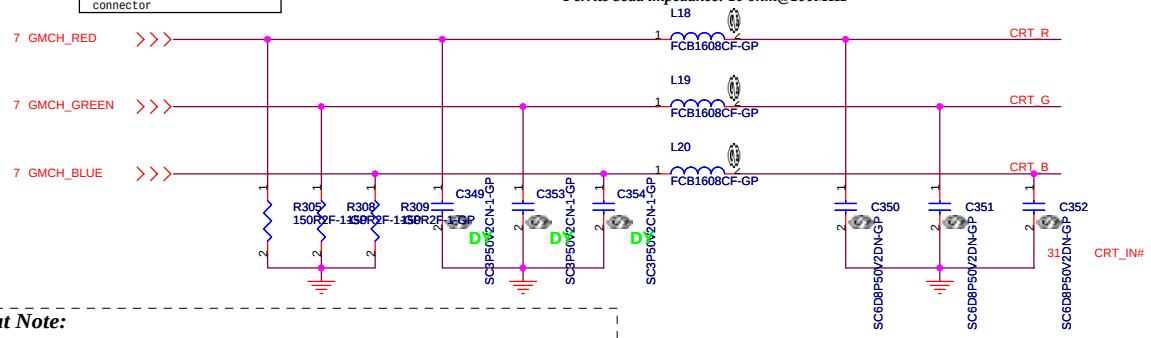
Size: Custom | Document Number: AG1 | Rev: -1

Date: Wednesday, January 18, 2006 | Sheet 13 of 45

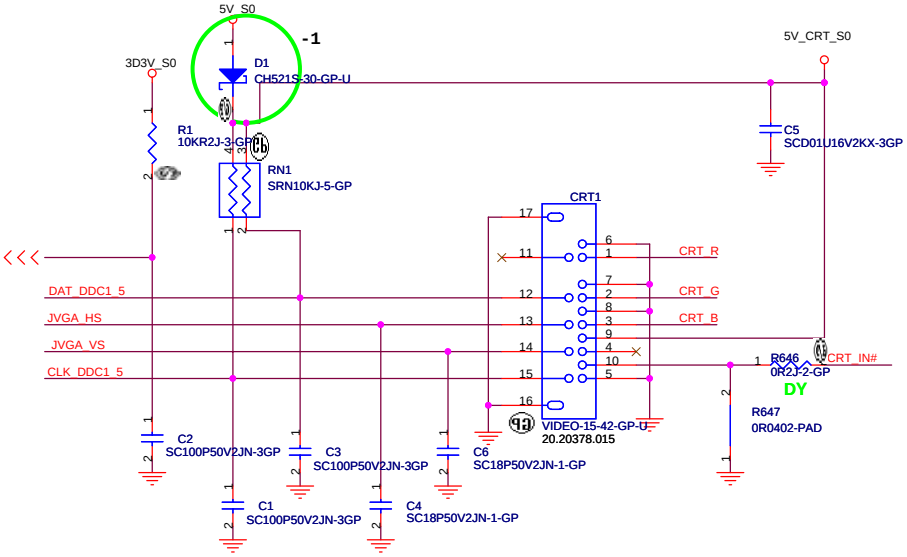
CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

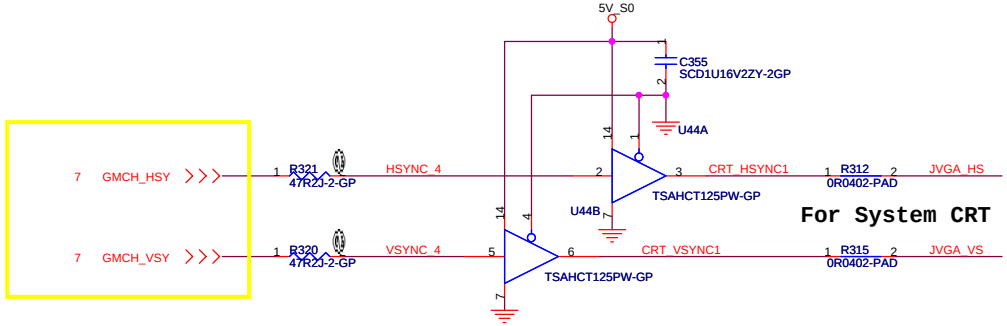
Ferrite bead impedance: 10 ohm@100MHz



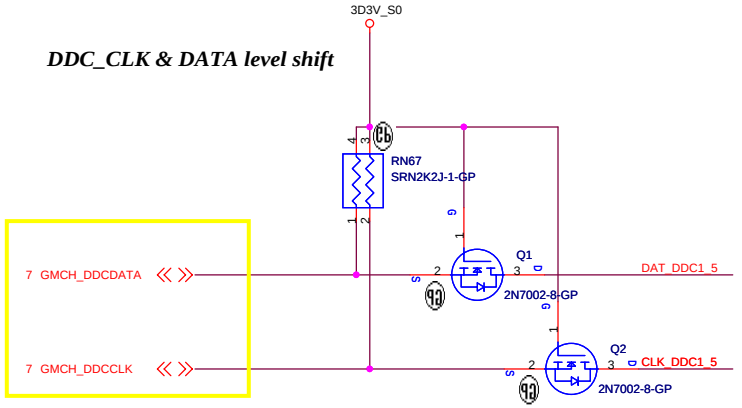
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



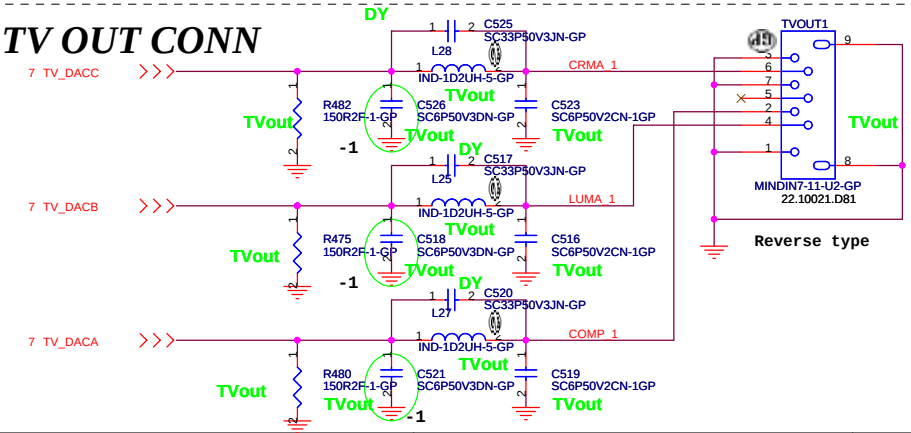
Hsync & Vsync level shift

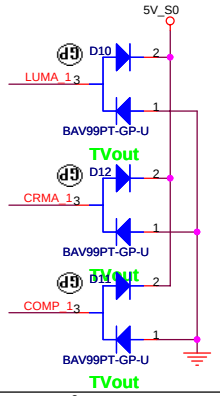


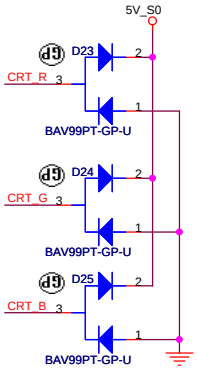
DDC_CLK & DATA level shift



TV OUT CONN







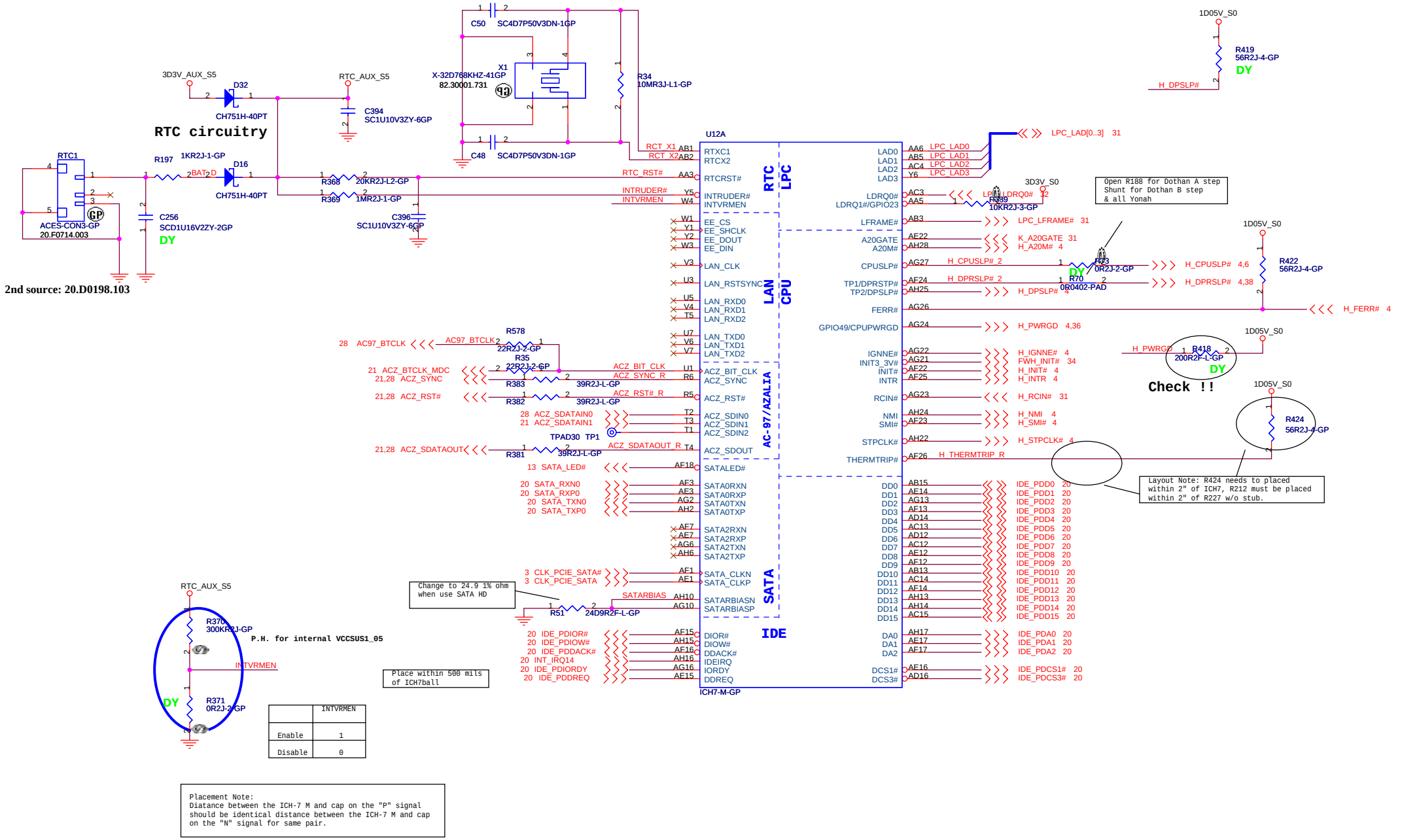
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CRT/TV Connector***

Size	Document Number	Rev
A3	AG1	-1

Date: Friday, February 24, 2006 Sheet 14 of 45



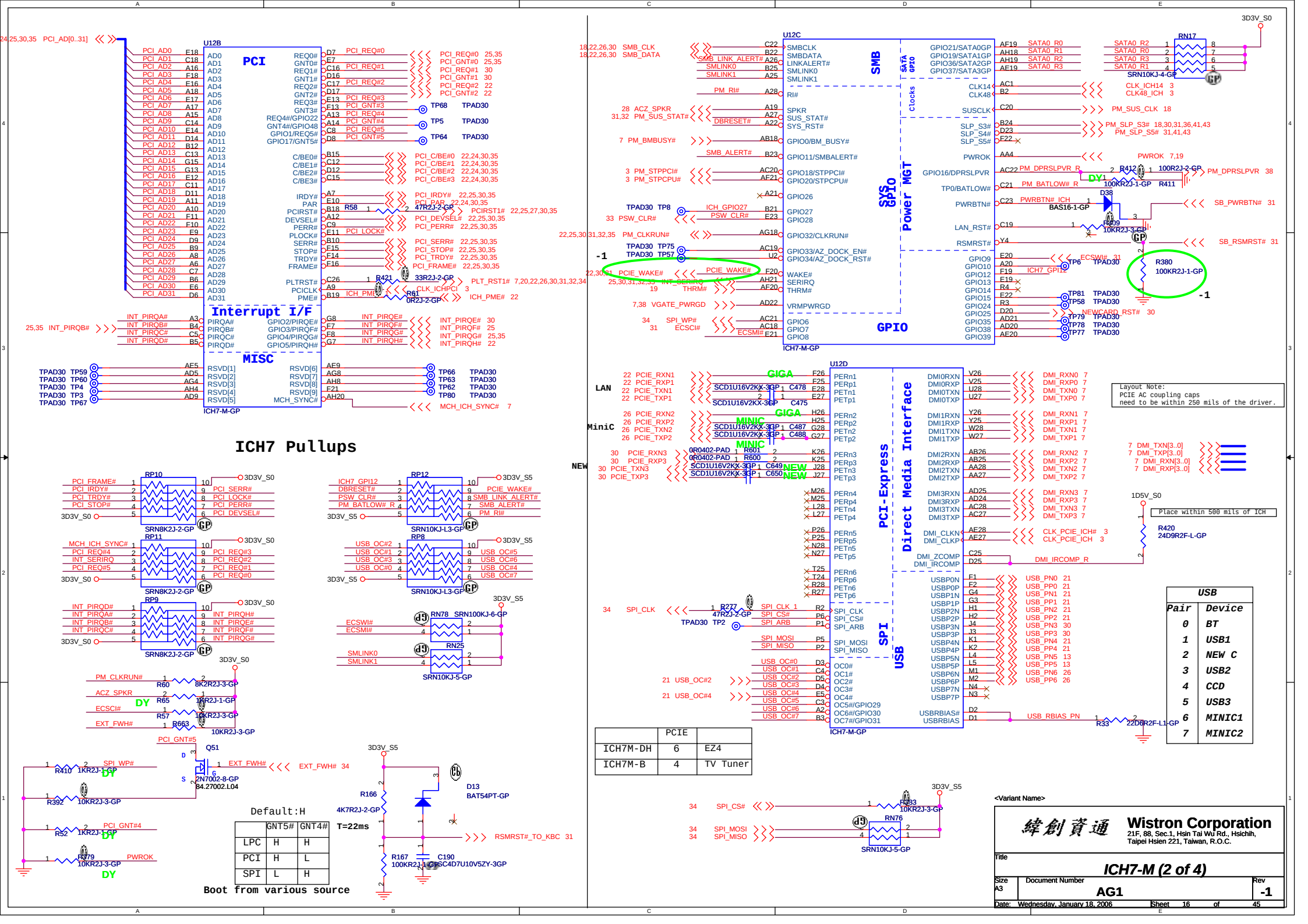
<Variant Name>

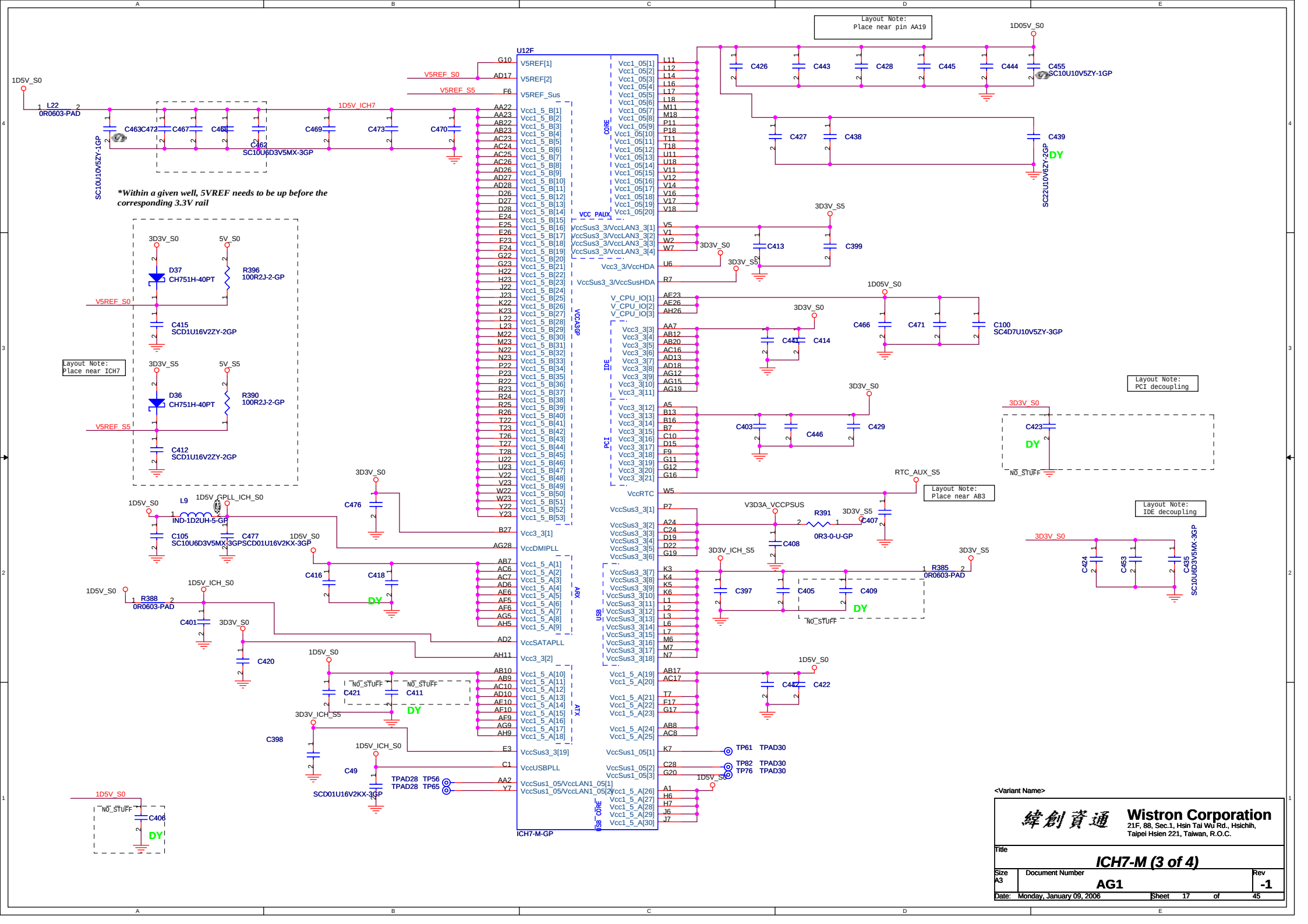
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

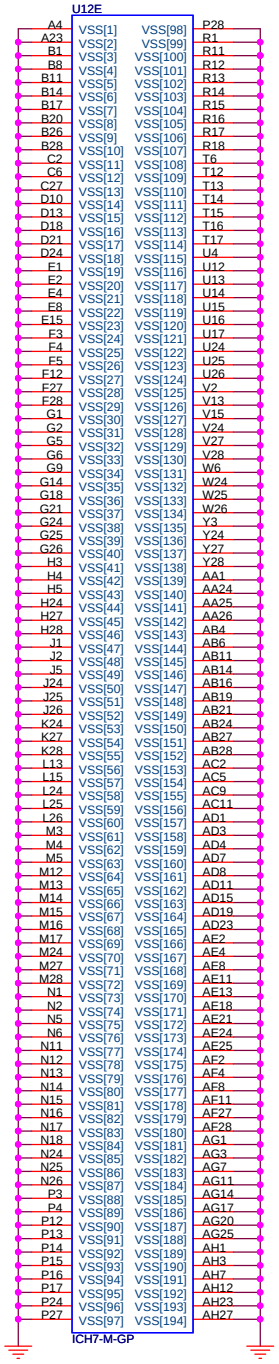
Title: ICH7-M (1 of 4)

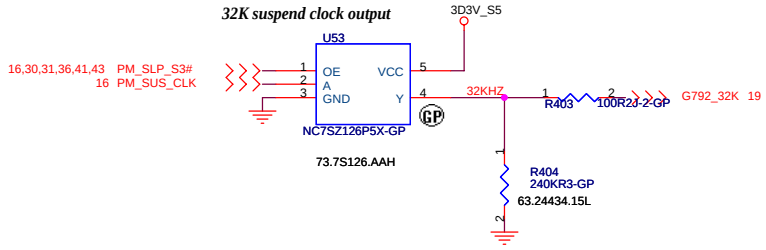
Size	Document Number	Rev
A3	AG1	-1

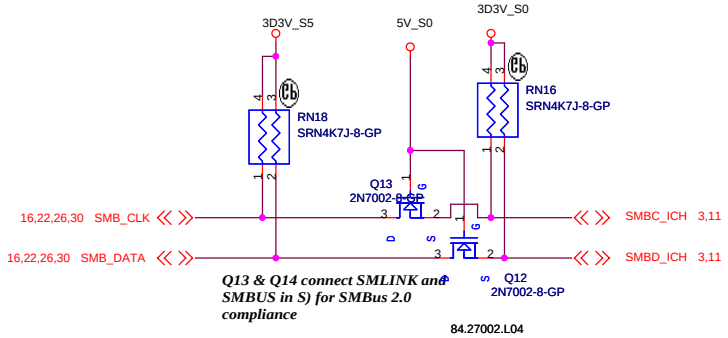
Date: Wednesday, January 18, 2006 Sheet 15 of 45


ICH7 Pullups
U12B
PCI
Interrupt I/F
MISC
ICH7-M-GP
U12C
SMB
GPIO
SYS MGT
Power MGT
Clocks
SATA GPIO
ICH7-M-GP
U12D
PCI-Express
Direct Media Interface
USB
SPI
ICH7-M-GP
LAN
MiniC
NEW
GIGA
MINIC
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Place within 500 mils of ICH
USB
Pair Device
0 BT
1 USB1
2 NEW C
3 USB2
4 CCD
5 USB3
6 MINIC1
7 MINIC2
PCIE
ICH7M-DH 6 EZ4
ICH7M-B 4 TV Tuner
Default:H
GNT5# GNT4#
LPC H H
PCI H L
SPI L H
Boot from various source
T=22ms
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (2 of 4)
Size A3
Document Number AG1
Rev -1
Date: Wednesday, January 18, 2006
Sheet 16 of 45


U12F
ICH7-M-GP
Layout Note:
Place near pin AA19
Layout Note:
Place near ICH7
Layout Note:
Place near AB3
Layout Note:
PCI decoupling
Layout Note:
IDE decoupling
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
1D5V_S0
3D3V_S0
5V_S0
3D3V_S5
5V_S5
V5REF_S0
V5REF_S5
1D5V_ICH7
1D5V_GPLL_ICH_S0
1D5V_ICH_S0
3D3V_ICH_S5
RTC_AUX_S5
V3D3A_VCCPSUS
L22
0R0603-PAD
SC10U10V5ZY-1GP
C463C472
C467
C468
C462
SC10U6D3V5MX-3GP
C469
C473
C470
D37
CH751H-40PT
R396
100R2J-2-GP
C415
SCD1U16V2ZY-2GP
D36
CH751H-40PT
R390
100R2J-2-GP
C412
SCD1U16V2ZY-2GP
L9
IND-1D2UH-5-GP
C105
SC10U6D3V5MX-3GP
C477
SCD01U16V2KX-3GP
C476
C416
C418
DY
R388
0R0603-PAD
C401
C420
C421
NO_STUFF
C411
C398
C49
SCD01U16V2KX-3GP
TPAD28
TP56
TPAD28
TP65
C406
C426
C443
C428
C445
C444
C455
SC10U10V5ZY-1GP
C427
C438
C439
SC22U10V6ZY-2GP
C413
C399
C466
C471
C100
SC4D7U10V5ZY-3GP
C441
C414
C403
C446
C429
C423
C424
C453
C435
SC10U6D3V5MX-3GP
R391
0R3-0-U-GP
C407
C408
C397
C405
C409
R385
0R0603-PAD
C442
C422
TP61
TPAD30
TP82
TP76
TPAD30
CORE
VCC_PAUX
VCCA3GP
IDE
PCI
AUX
USB
AXK
CSB CORE
Vcc1_05[1]
Vcc1_05[2]
Vcc1_05[3]
Vcc1_05[4]
Vcc1_05[5]
Vcc1_05[6]
Vcc1_05[7]
Vcc1_05[8]
Vcc1_05[9]
Vcc1_05[10]
Vcc1_05[11]
Vcc1_05[12]
Vcc1_05[13]
Vcc1_05[14]
Vcc1_05[15]
Vcc1_05[16]
Vcc1_05[17]
Vcc1_05[18]
Vcc1_05[19]
Vcc1_05[20]
VccSus3_3/VccLAN3_3[1]
VccSus3_3/VccLAN3_3[2]
VccSus3_3/VccLAN3_3[3]
VccSus3_3/VccLAN3_3[4]
Vcc3_3/VccHDA
VccSus3_3/VccSusHDA
V_CPU_IO[1]
V_CPU_IO[2]
V_CPU_IO[3]
Vcc3_3[1]
VccDMIPLL
Vcc1_5_A[1]
Vcc1_5_A[2]
Vcc1_5_A[3]
Vcc1_5_A[4]
Vcc1_5_A[5]
Vcc1_5_A[6]
Vcc1_5_A[7]
Vcc1_5_A[8]
Vcc1_5_A[9]
VccSATAPLL
Vcc3_3[2]
Vcc1_5_A[10]
Vcc1_5_A[11]
Vcc1_5_A[12]
Vcc1_5_A[13]
Vcc1_5_A[14]
Vcc1_5_A[15]
Vcc1_5_A[16]
Vcc1_5_A[17]
Vcc1_5_A[18]
VccSus3_3[19]
VccUSBPLL
VccSus1_05/VccLAN1_05[1]
VccSus1_05/VccLAN1_05[2]
Vcc3_3[3]
Vcc3_3[4]
Vcc3_3[5]
Vcc3_3[6]
Vcc3_3[7]
Vcc3_3[8]
Vcc3_3[9]
Vcc3_3[10]
Vcc3_3[11]
Vcc3_3[12]
Vcc3_3[13]
Vcc3_3[14]
Vcc3_3[15]
Vcc3_3[16]
Vcc3_3[17]
Vcc3_3[18]
Vcc3_3[19]
Vcc3_3[20]
Vcc3_3[21]
VccRTC
VccSus3_3[1]
VccSus3_3[2]
VccSus3_3[3]
VccSus3_3[4]
VccSus3_3[5]
VccSus3_3[6]
VccSus3_3[7]
VccSus3_3[8]
VccSus3_3[9]
VccSus3_3[10]
VccSus3_3[11]
VccSus3_3[12]
VccSus3_3[13]
VccSus3_3[14]
VccSus3_3[15]
VccSus3_3[16]
VccSus3_3[17]
VccSus3_3[18]
Vcc1_5_A[19]
Vcc1_5_A[20]
Vcc1_5_A[21]
Vcc1_5_A[22]
Vcc1_5_A[23]
Vcc1_5_A[24]
Vcc1_5_A[25]
VccSus1_05[1]
VccSus1_05[2]
VccSus1_05[3]
Vcc1_5_A[26]
Vcc1_5_A[27]
Vcc1_5_A[28]
Vcc1_5_A[29]
Vcc1_5_A[30]
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (3 of 4)
Size
A3
Document Number
AG1
Rev
-1
Date: Monday, January 09, 2006
Sheet 17 of 45







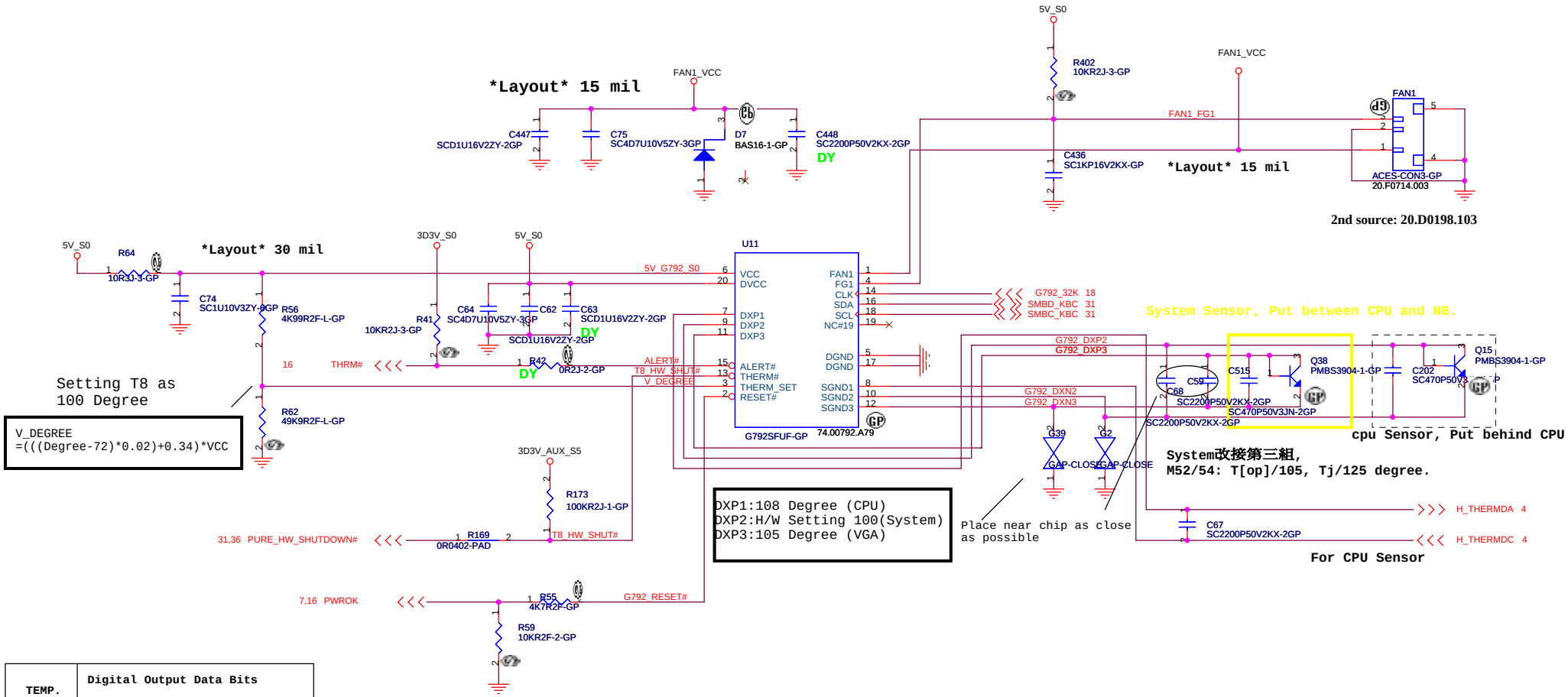
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ICH7-M (4 of 4)/ODD***

Size	Document Number	Rev
A3	AG1	-1

Date: Wednesday, January 18, 2006 Sheet 18 of 45



TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

<Variant Name>

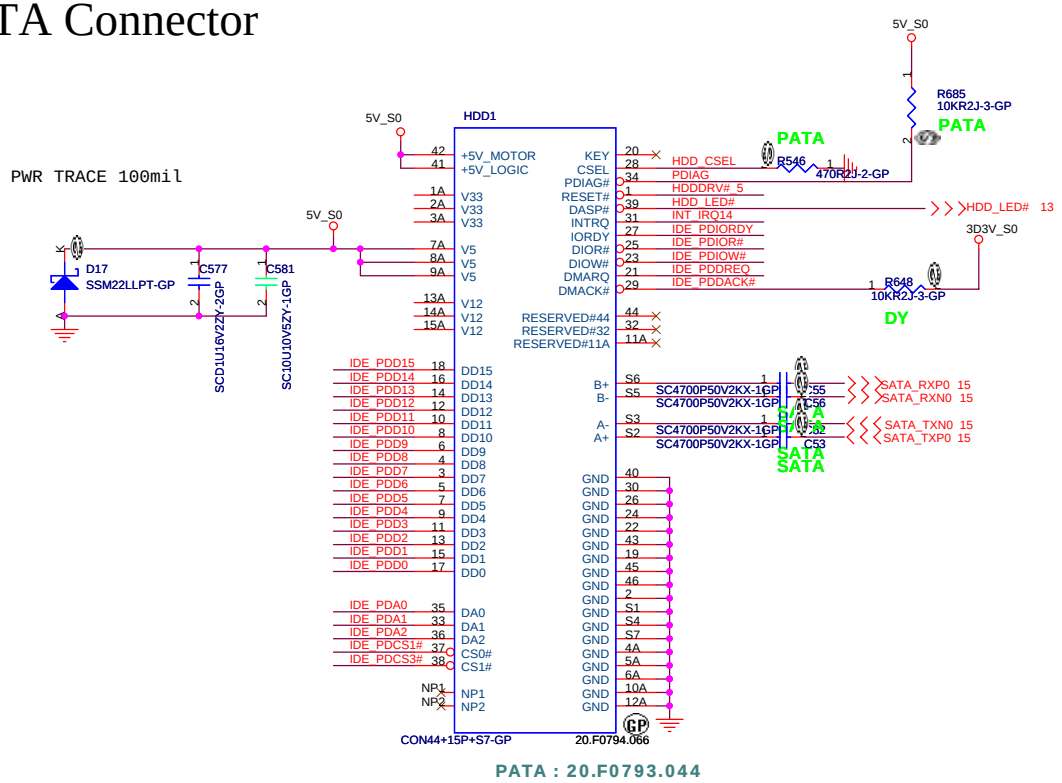
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor G792

Size	Document Number	Rev
Custom	AG1	-1

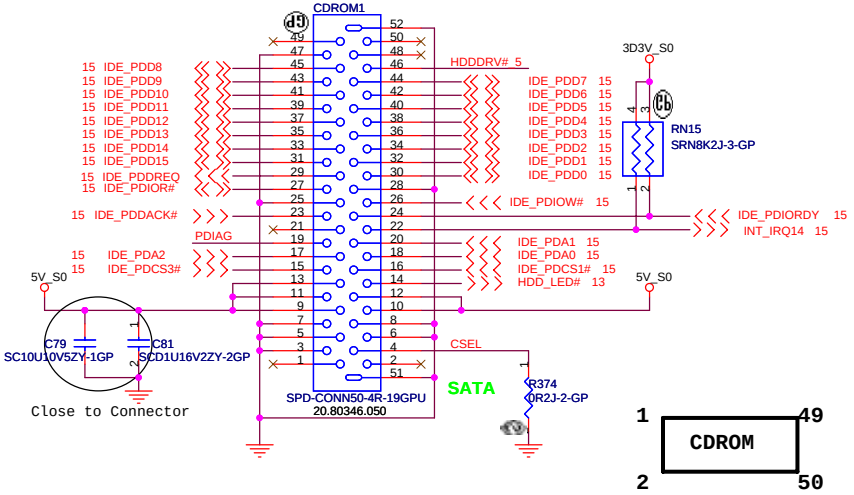
Date: Wednesday, January 18, 2006 Sheet 19 of 45

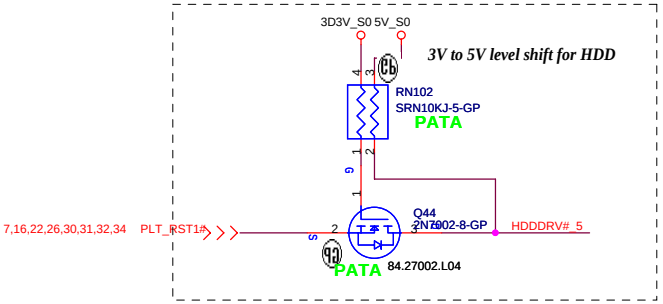
SATA Connector



PATA : 20.F0793.044

CDROM Connector





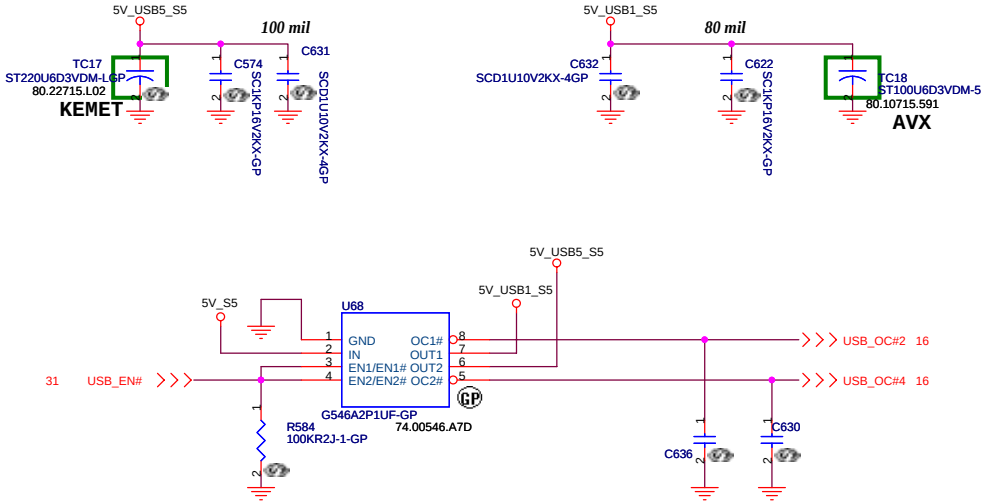
<variant_name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

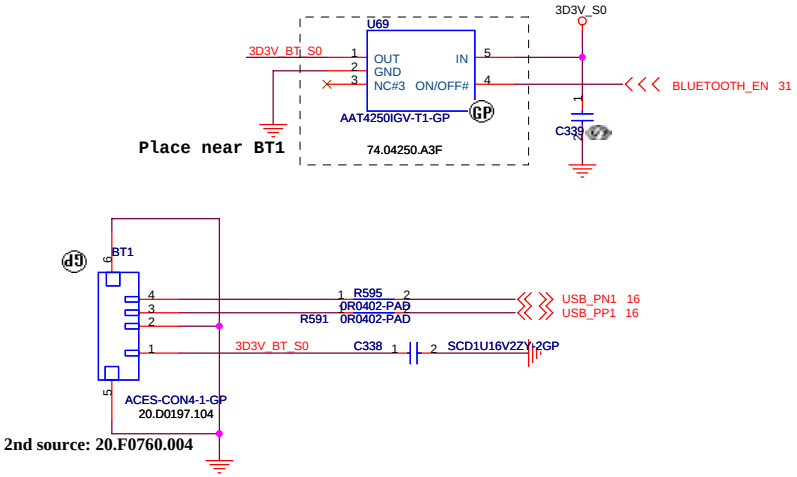
Title: SATA/PATA HDD ULi-M5285

Size	Document Number	Rev
A3	AG1	-1

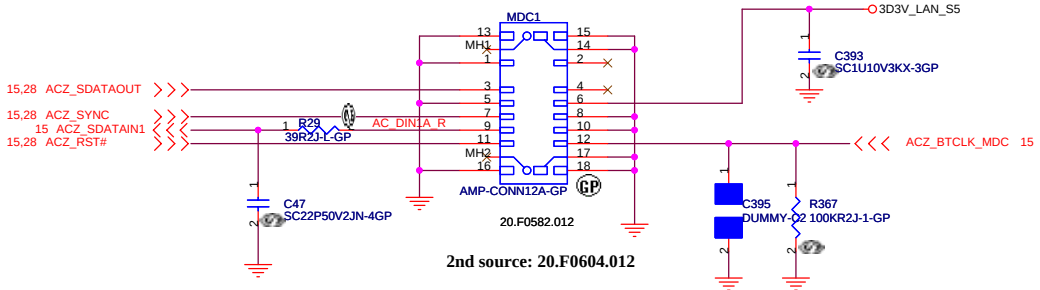
Date: Wednesday, January 18, 2006 Sheet 20 of 45



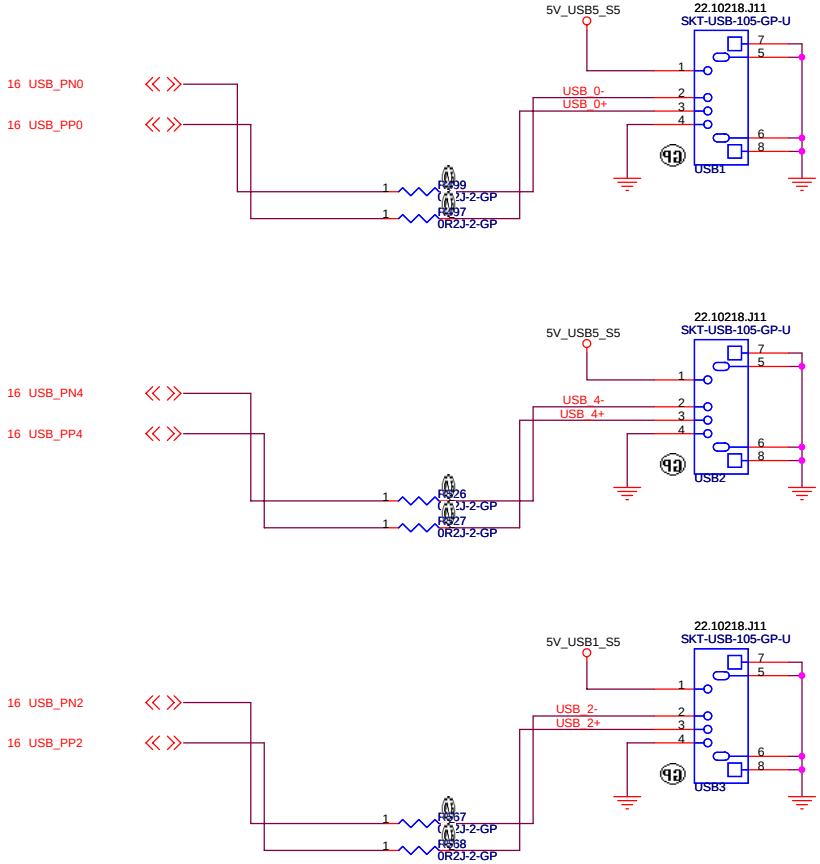
BLUETOOTH MODULE CONNECTOR



MDC 1.5 CONN



USB PORT



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB and MDC I/F

Size	Document Number	Rev
A3	AG1	-1

Date: Friday, February 24, 2006 Sheet 21 of 45

Broadcom LAN
BCM4401E
BCM5789
BCM5787M

IDSEL:AD23
INTA-->:INT_PIRQH#
GNT:PCI_GNT#2
REQ:PCI_REQ#2

"GIGA" -- stuff when 5789 and 5787M.
"4401E" -- stuff when 4401E.
"5789" -- stuff when 5789.
"5787" -- stuff when 5787.
"no 5787" -- stuff when 4401E and 5789.

R79 :1.27K 1% FOR BCM4401E -> 64.12715.L01
1.24K 1% FOR BCM5789 -> 64.12415.6DL

CLOSE TO GPHY PINS

Place PLLVDD/AVDDL CKT as close to chip as possible

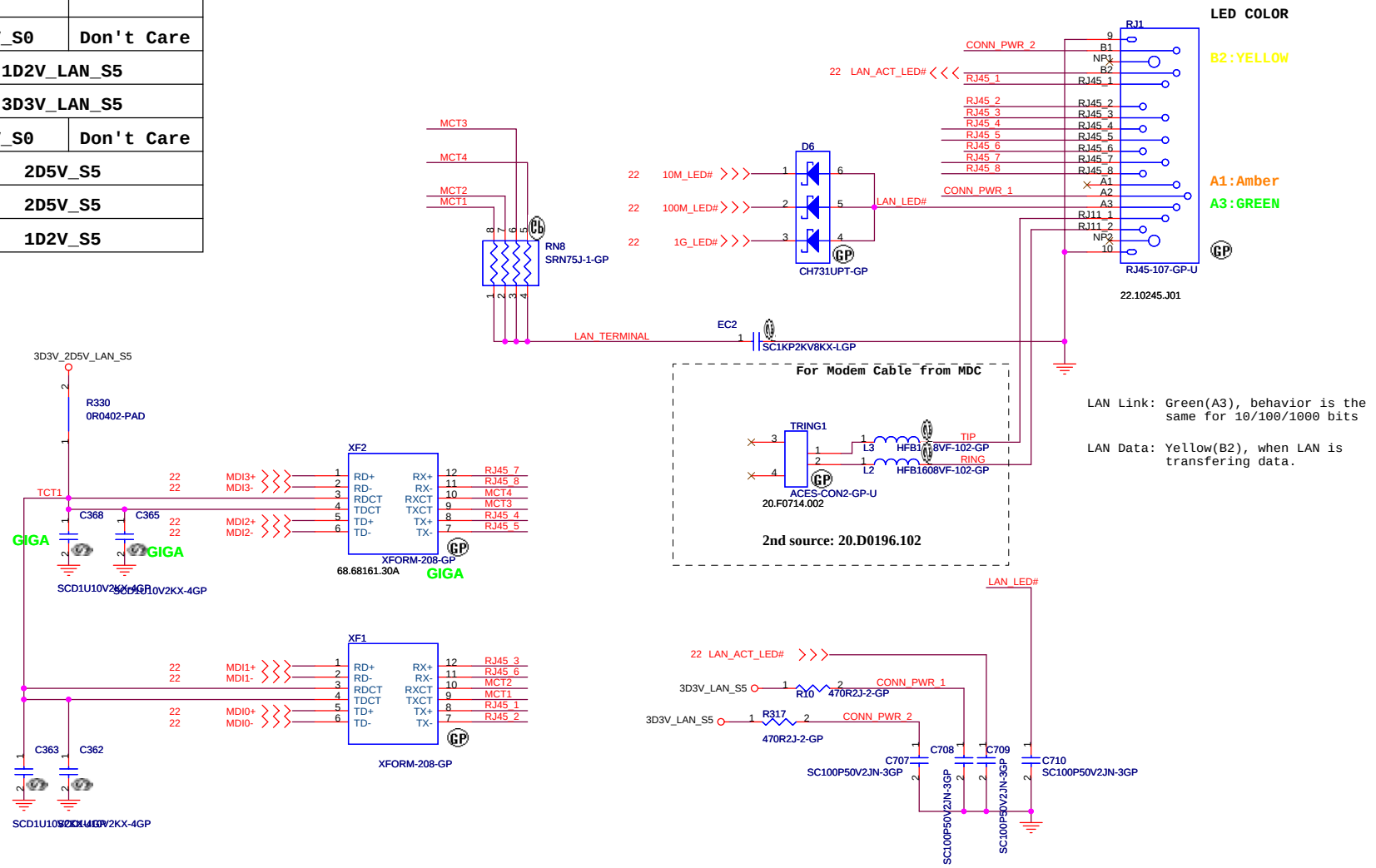
BCM4401EKFBG-GP

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BCM4401E / BCM5789
Size: A3 | Document Number: AG1 | Rev: -1
Date: Wednesday, January 18, 2006 | Sheet 22 of 45

LAN Connector

Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

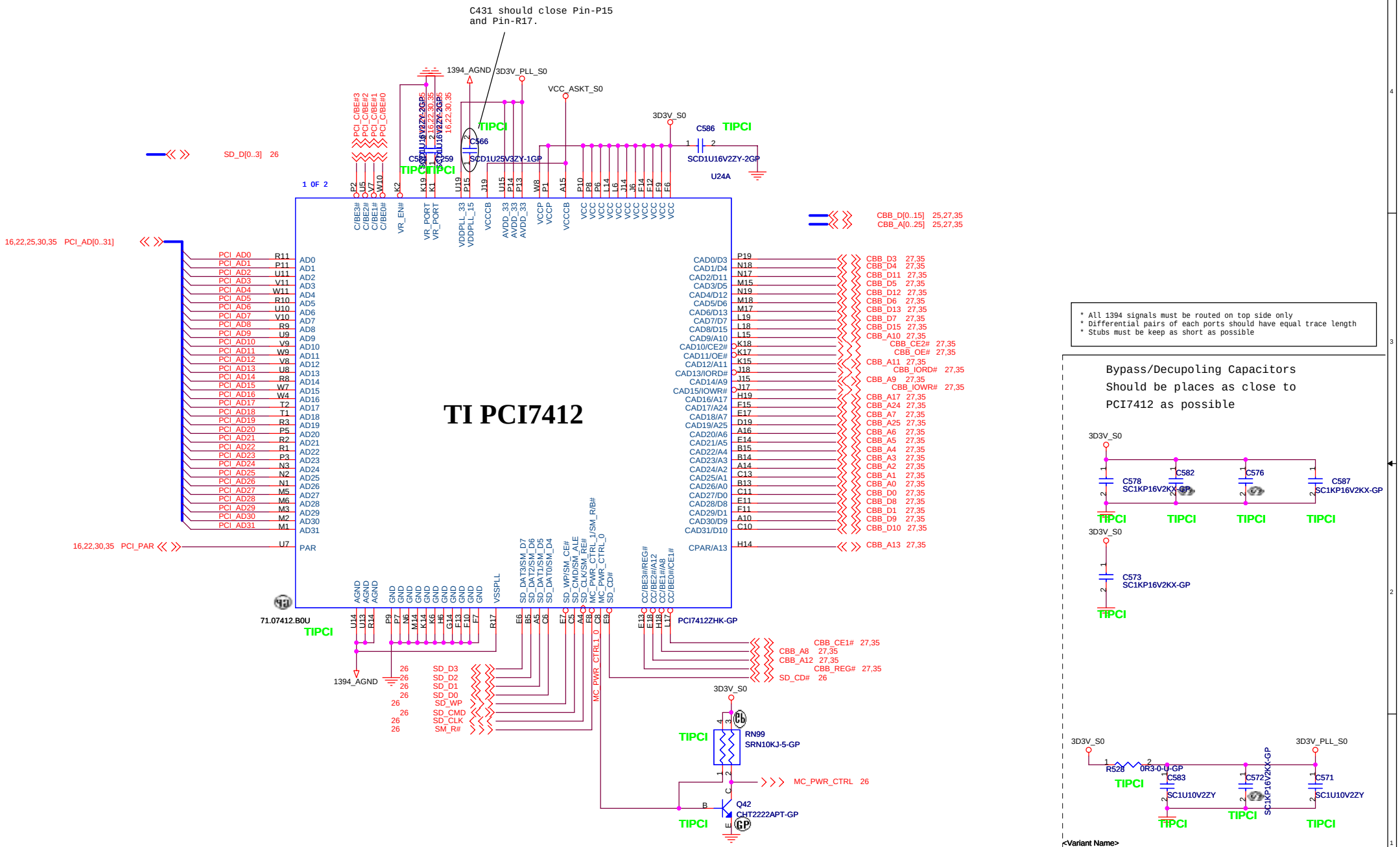
<Variant Name>

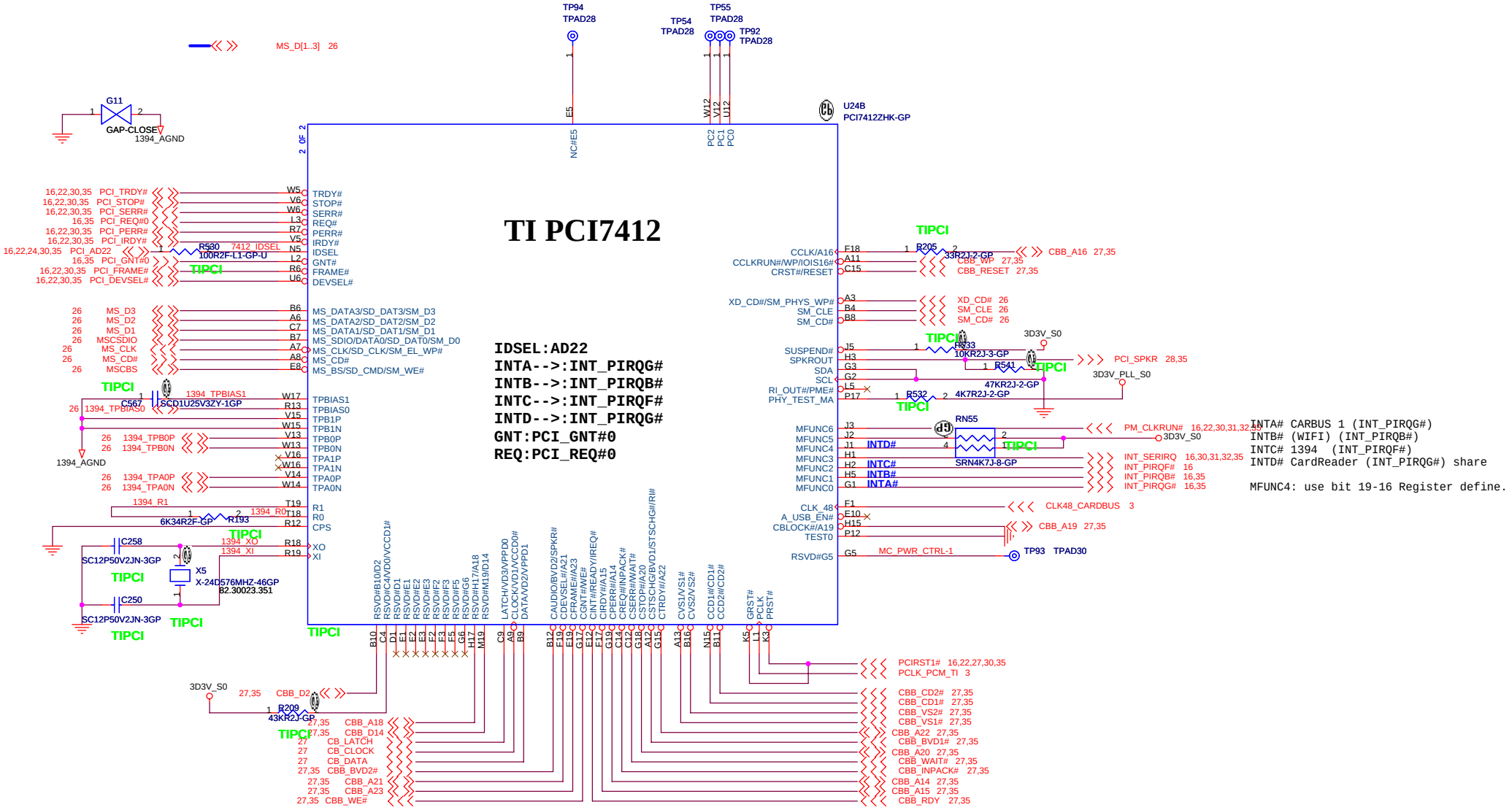
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

Size	Document Number	Rev
A3	AG1	-1

Date: Wednesday, January 18, 2006 Sheet 23 of 45


C431 should close Pin-P15
and Pin-R17.
TI PCI7412
1 0F 2
71.07412.B0U
PCI7412ZHK-GP
SD_D[0..3] 26
16,22,25,30,35 PCI_AD[0..31]
16,22,30,35 PCI_PAR
CBB_D[0..15] 25,27,35
CBB_A[0..25] 25,27,35
1394_AGND
3D3V_PLL_S0
VCC_ASKT_S0
3D3V_S0
SCD1U16V2ZY-2GP
SCD1U25V3ZY-1GP
U24A
RN99
SRN10KJ-5-GP
Q42
CHT2222APT-GP
MC_PWR_CTRL 26
SD_CD# 26
CBB_CE1# 27,35
CBB_A8 27,35
CBB_A12 27,35
CBB_REG# 27,35
* All 1394 signals must be routed on top side only
* Differential pairs of each ports should have equal trace length
* Stubs must be keep as short as possible
Bypass/Decupoling Capacitors
Should be places as close to
PCI7412 as possible
C578 SC1KP16V2KX-GP
C582
C576
C587 SC1KP16V2KX-GP
C573 SC1KP16V2KX-GP
R528 0R3-0-U-GP
C583 SC1U10V2ZY
C572 SC1KP16V2KX-GP
C571 SC1U10V2ZY
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TI PCI7412 (1 of 2)
Size A3
Document Number AG1
Rev -1
Date: Wednesday, January 18, 2006
Sheet 24 of 45



<Variant Name>

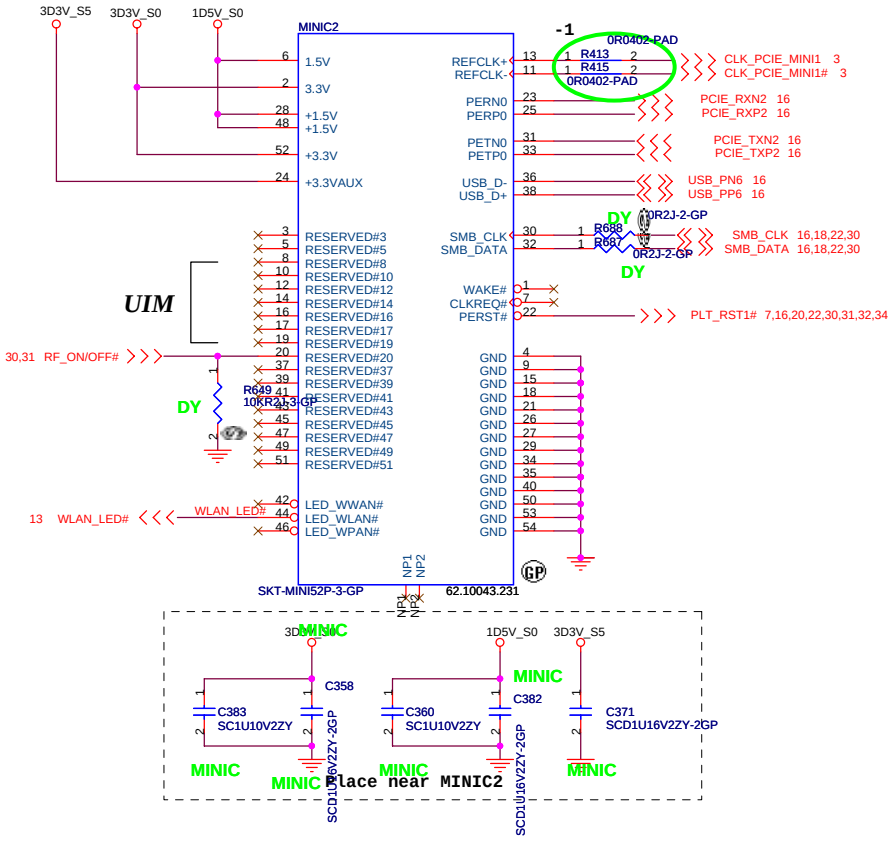
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

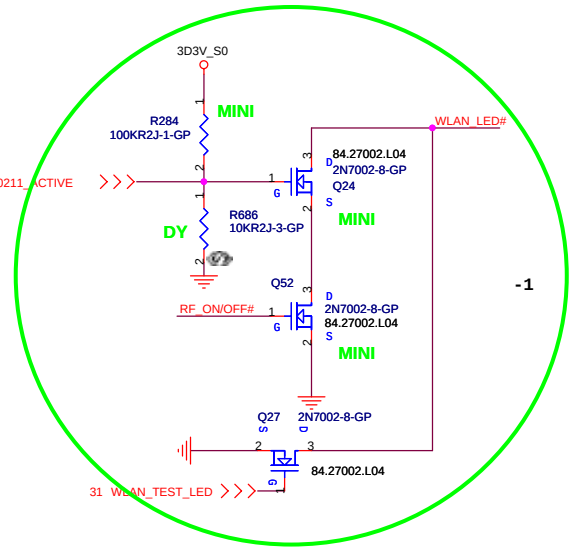
Title: *TI PCI7412 (2 of 2)*

Size	Document Number	Rev
A3	AG1	-1

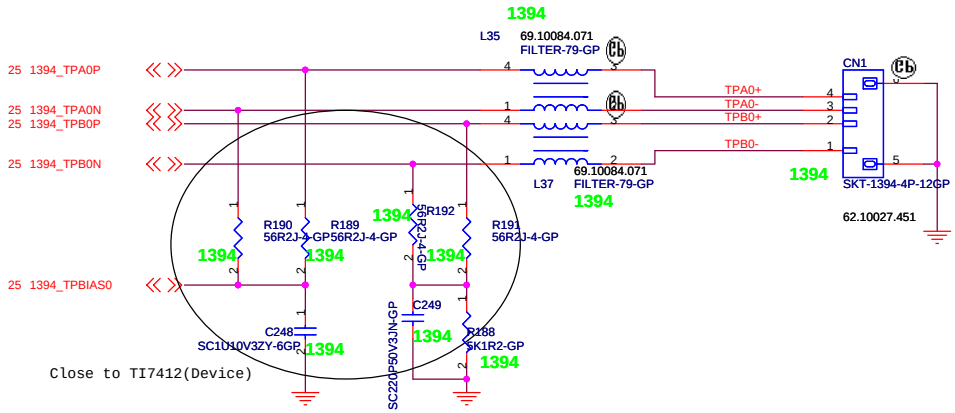
Date: Wednesday, January 18, 2006 Sheet 25 of 45

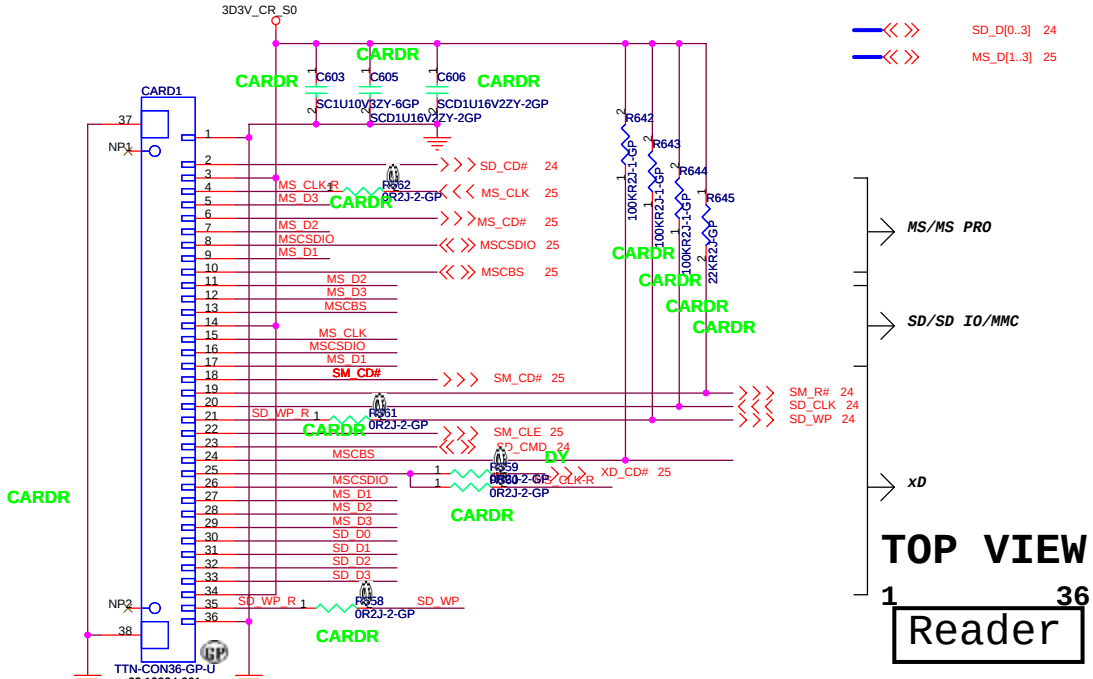
Mini Card Connector

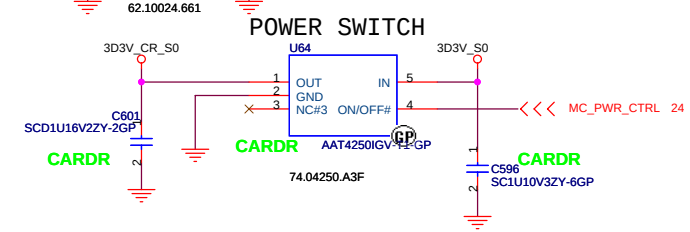




1394 Connector







緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

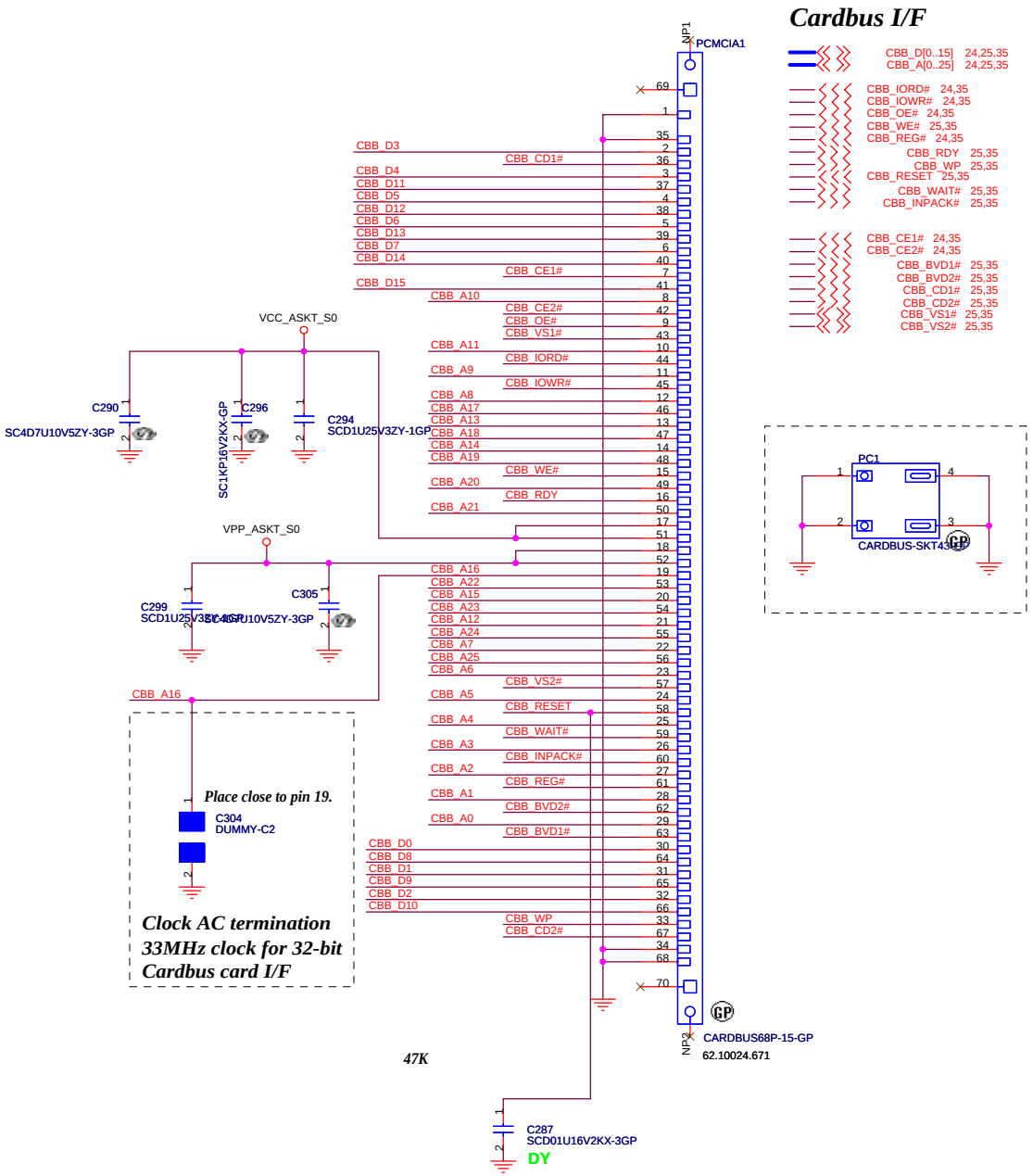
<variant_name>

Title: MINI CARD / 1394

Size	Document Number	Rev
A3	AG1	-1

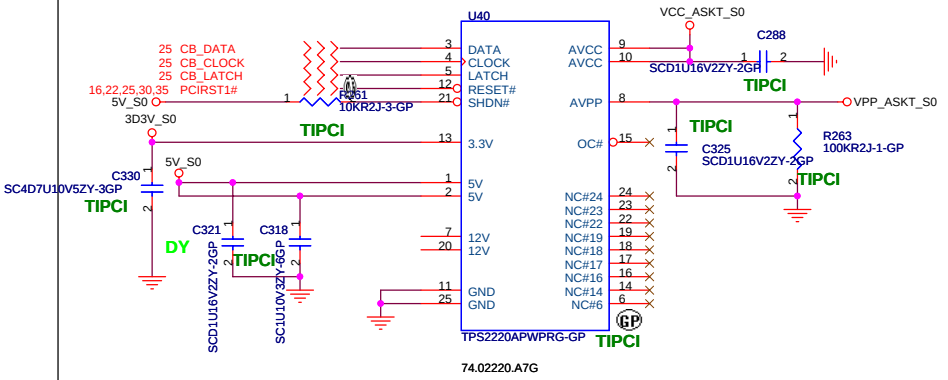
Date: Wednesday, March 01, 2006 Sheet 26 of 45

PCMCIA Socket

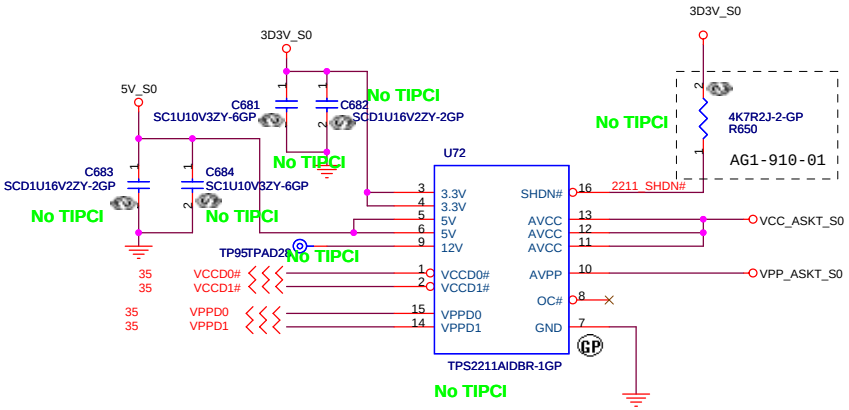


Cardbus I/F

TI Power switch



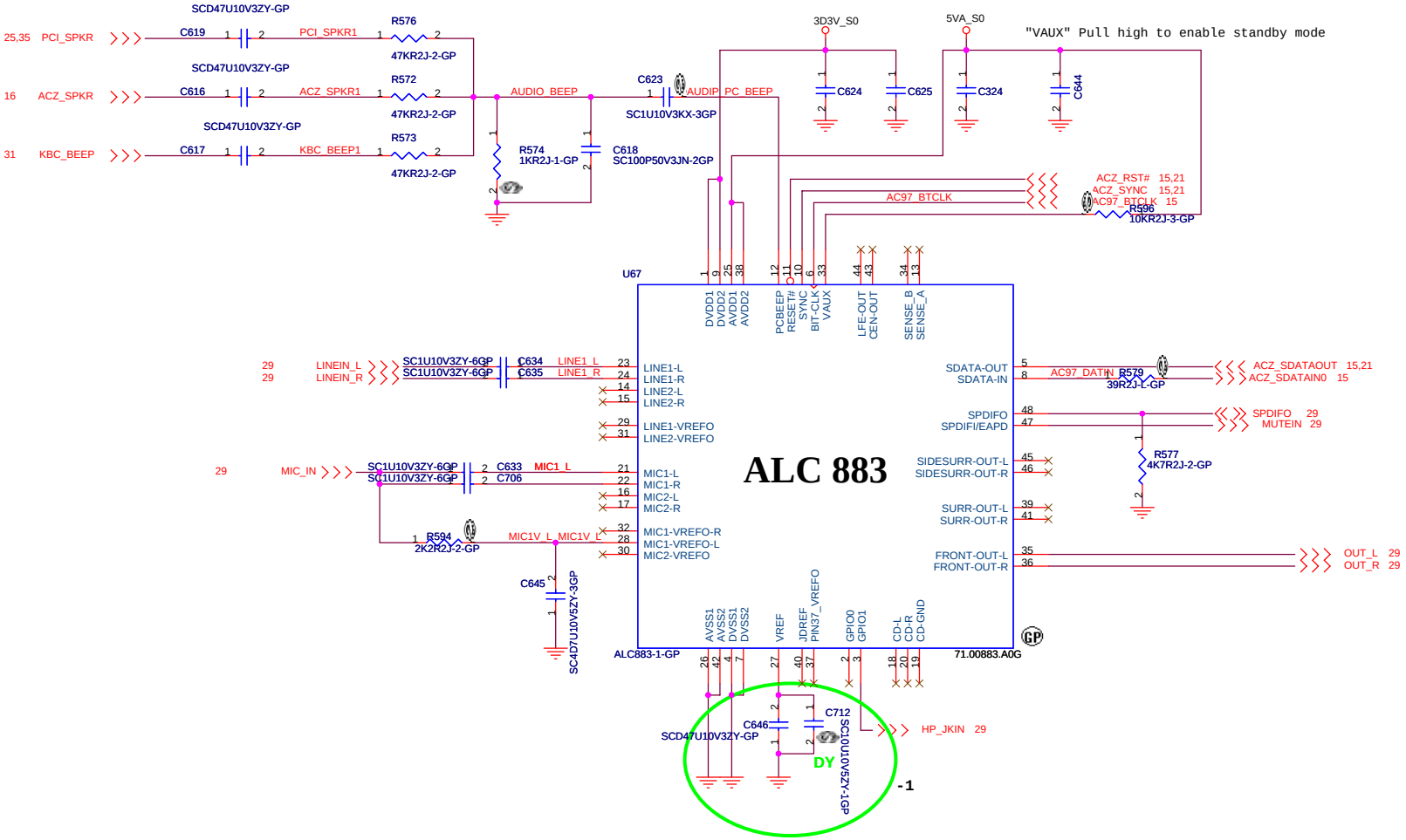
ENE Power switch



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

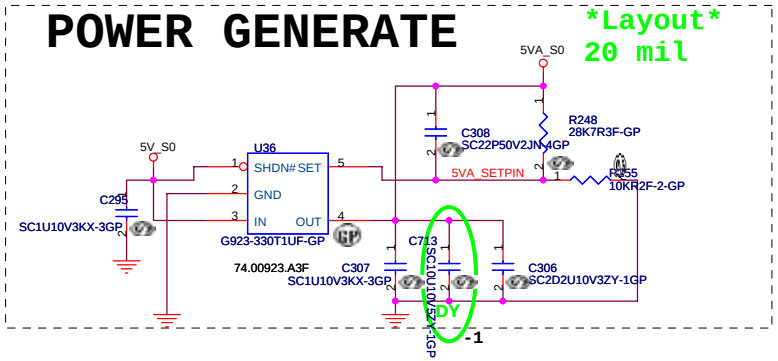
Title	PCMCIA	
Size A3	Document Number AG1	Rev -1
Date: Friday, February 24, 2006	Sheet 27 of 45	



1) When GPIO0 is assered, AMP should be muted.
2) SPDIFO should be turned off when not used.

Configuation:
(3 External Jacks, 1 internal Mic, 1 stereo output Speaker Amp.

Pin	Symbol	Location	Re-tasking
35/36	FRONT	AMP,Jack1	AMP output, line input
39/41	SURR	X	X
43/44	CEN/LEFT	X	SURR-VREFO-L/R
45/46	SIDESURR	X	SIDESURR-L is MIC2-VREFO-R, SIDESURR-R is LINE2-VREFO-R
23/24	LINE1	Jack 2	Line input, line output
21/22	MIC1	Jack 3	Mic input, line output
14/15	LINE2	X	X
16/17	MIC2	Int. Mic	Mic input



<Variant Name>

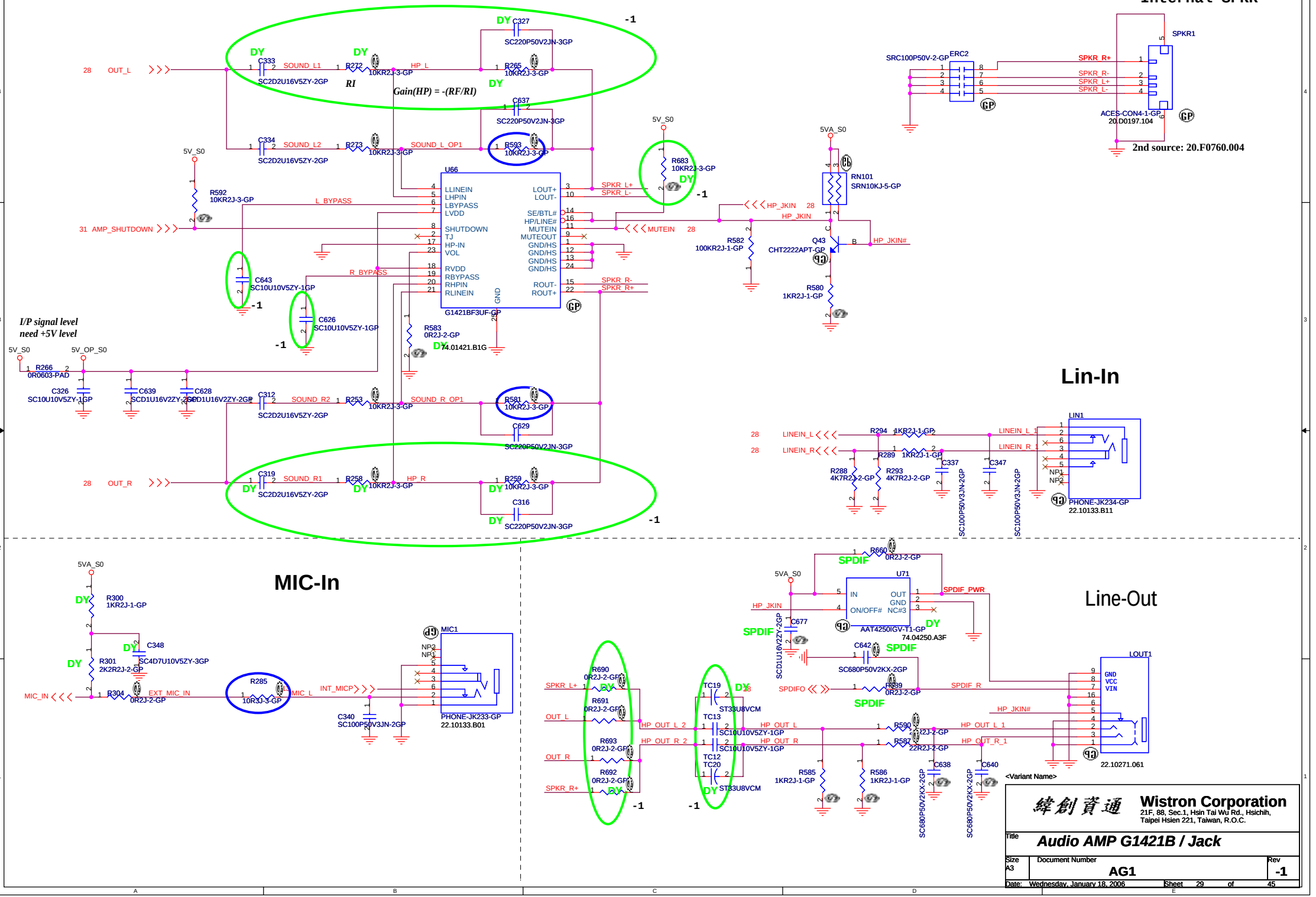
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Azalia codec ALC883

Size	Document Number	Rev
A3	AG1	-1

Date: Wednesday, January 18, 2006 Sheet 28 of 45

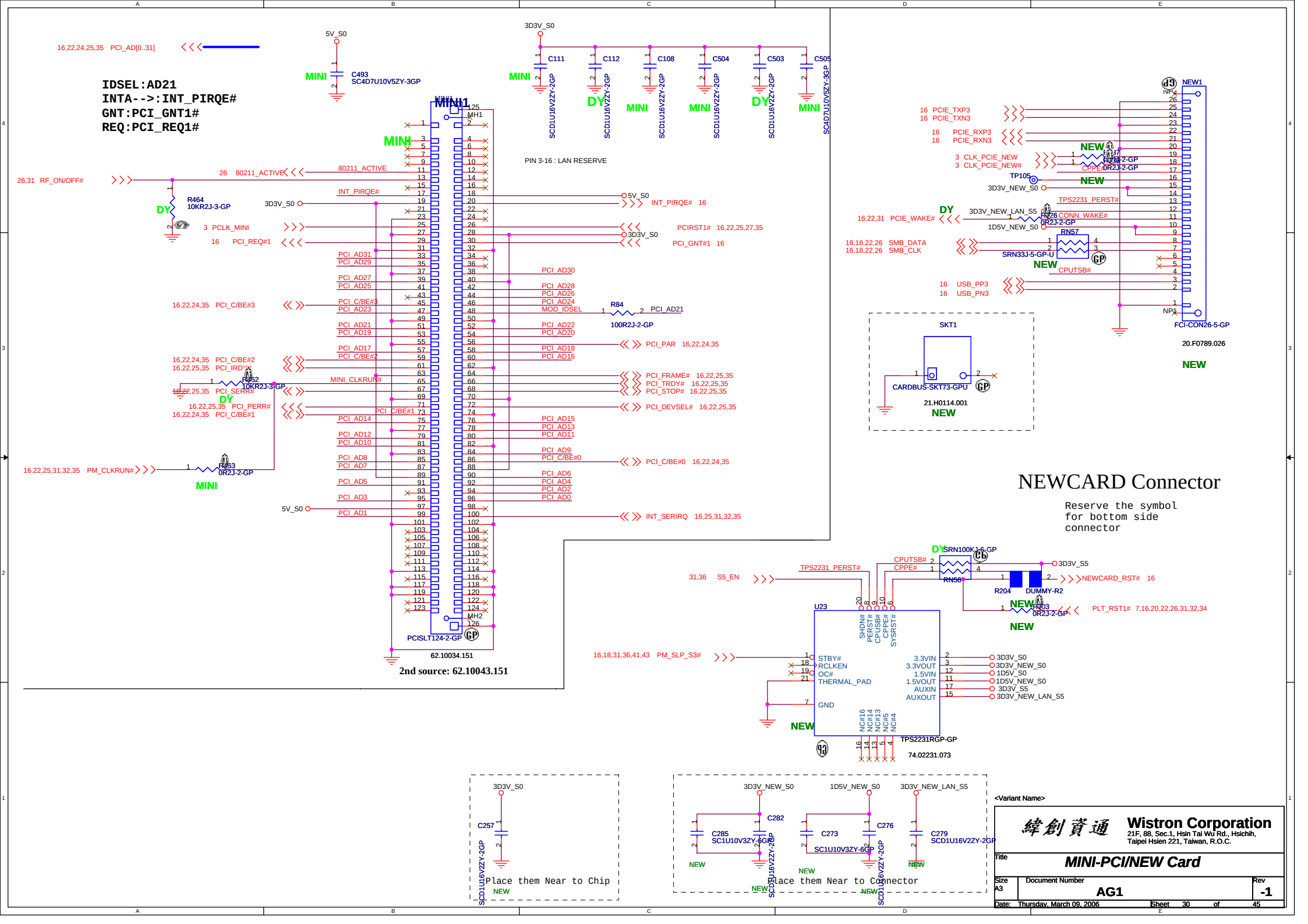
AUDIO OP AMPLIFIER

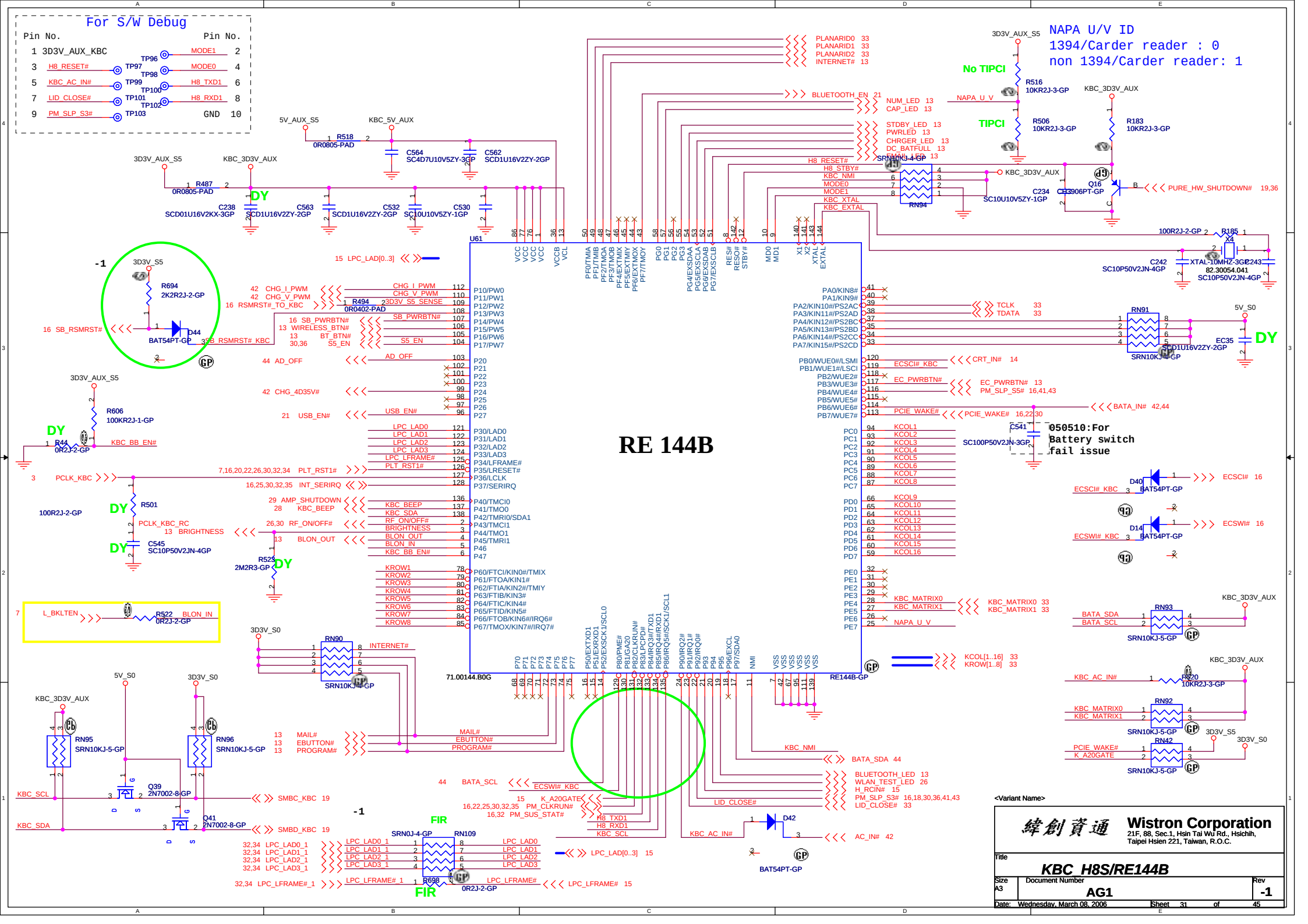


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Audio AMP G1421B / Jack	
Size A3	Document Number AG1	Rev -1
Date: Wednesday, January 18, 2006	Sheet 29 of 45	

<variant_name>
</variant_name>


IDSEL:AD21
INTA-->:INT_PIRQE#
GNT:PCI_GNT1#
REQ:PCI_REQ1#
16,22,24,25,35 PCI_AD[0..31]
5V_S0
MINI
C493
SC4D7U10V5ZY-3GP
3D3V_S0
C111
C112
C108
C504
C503
C505
SCD1U16V2ZY-2GP
SC4D7U10V5ZY-3GP
DY
PIN 3-16 : LAN RESERVE
MINI1
MH1
MH2
PCISLT124-2-GP
62.10034.151
2nd source: 62.10043.151
26,31 RF_ON/OFF#
R464
10KR2J-3-GP
26 80211_ACTIVE
80211_ACTIVE
INT_PIRQE#
INT_PIRQE# 16
3 PCLK_MINI
16 PCI_REQ#1
PCIRST1# 16,22,25,27,35
PCI_GNT#1 16
PCI_AD31
PCI_AD29
PCI_AD27
PCI_AD25
PCI_C/BE#3
PCI_AD23
PCI_AD21
PCI_AD19
PCI_AD17
PCI_C/BE#2
PCI_IRDY#
PCI_SERR#
PCI_PERR#
PCI_C/BE#1
PCI_AD14
PCI_AD12
PCI_AD10
PCI_AD8
PCI_AD7
PCI_AD5
PCI_AD3
PCI_AD1
PCI_AD30
PCI_AD28
PCI_AD26
PCI_AD24
MOD_IDSEL
PCI_AD22
PCI_AD20
PCI_AD18
PCI_AD16
PCI_AD15
PCI_AD13
PCI_AD11
PCI_AD9
PCI_C/BE#0
PCI_AD6
PCI_AD4
PCI_AD2
PCI_AD0
R84
100R2J-2-GP
PCI_PAR 16,22,24,35
PCI_FRAME# 16,22,25,35
PCI_TRDY# 16,22,25,35
PCI_STOP# 16,22,25,35
PCI_DEVSEL# 16,22,25,35
PCI_C/BE#0 16,22,24,35
INT_SERIRQ 16,25,31,32,35
MINI_CLKRUN#
R462
10KR2J-3-GP
R463
0R2J-2-GP
16,22,25,31,32,35 PM_CLKRUN#
16 PCIE_TXP3
16 PCIE_TXN3
16 PCIE_RXP3
16 PCIE_RXN3
3 CLK_PCIE_NEW
3 CLK_PCIE_NEW#
TP105
3D3V_NEW_S0
TPS2231_PERST#
16,22,31 PCIE_WAKE#
3D3V_NEW_LAN_S5
CONN_WAKE#
1D5V_NEW_S0
RN57
SRN33J-5-GP-U
16,18,22,26 SMB_DATA
16,18,22,26 SMB_CLK
CPUTSB#
16 USB_PP3
16 USB_PN3
NEW1
FCI-CON26-5-GP
20.F0789.026
SKT1
CARDBUS-SKT73-GPU
21.H0114.001
NEWCARD Connector
Reserve the symbol
for bottom side
connector
SRN100K1-6-GP
RN56
CPPE#
R204
DUMMY-R2
NEWCARD_RST# 16
PLT_RST1# 7,16,20,22,26,31,32,34
31,36 S5_EN
U23
SHDN#
PERST#
CPUSB#
CPPE#
SYSRST#
STBY#
RCLKEN
OC#
THERMAL_PAD
GND
3.3VIN
3.3VOUT
1.5VIN
1.5VOUT
AUXIN
AUXOUT
3D3V_S0
3D3V_NEW_S0
1D5V_S0
1D5V_NEW_S0
3D3V_S5
3D3V_NEW_LAN_S5
16,18,31,36,41,43 PM_SLP_S3#
TPS2231RGP-GP
74.02231.073
C257
Place them Near to Chip
C282
C285
SC1U10V3ZY-6GP
C273
C276
C279
SCD1U16V2ZY-2GP
Place them Near to Connector
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
MINI-PCI/NEW Card
Size A3
Document Number AG1
Rev -1
Date: Thursday, March 09, 2006
Sheet 30 of 45

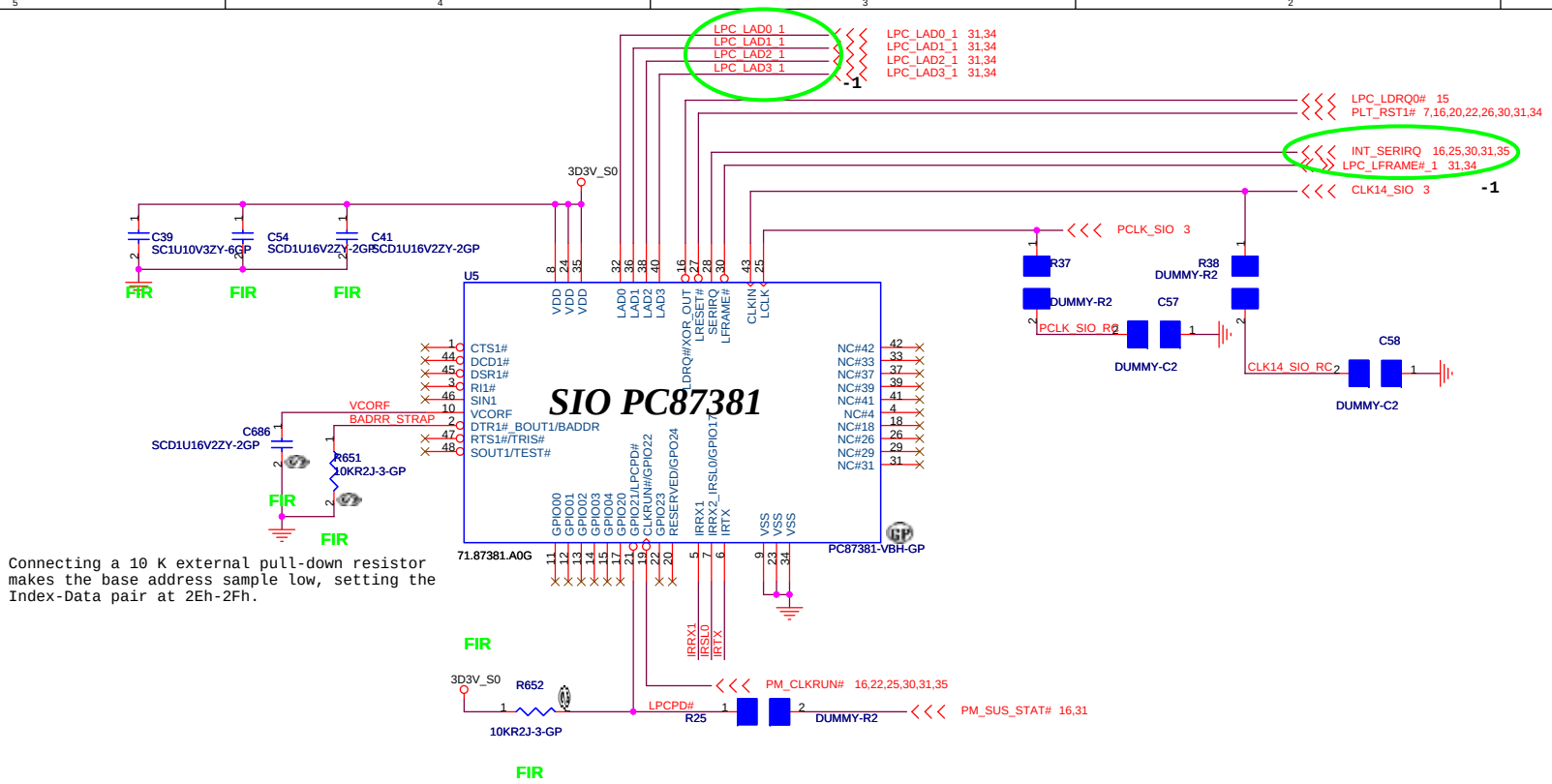


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC_H8S/RE144B

Size	Document Number	Rev
A3	AG1	-1

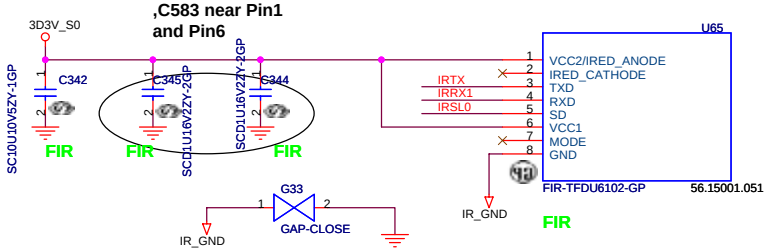
Date: Wednesday, March 08, 2006 Sheet 31 of 45



VISHAY FIR/CIR Module

Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close to U32

Place C581 ,C583 near Pin1 and Pin6



<Variant Name>

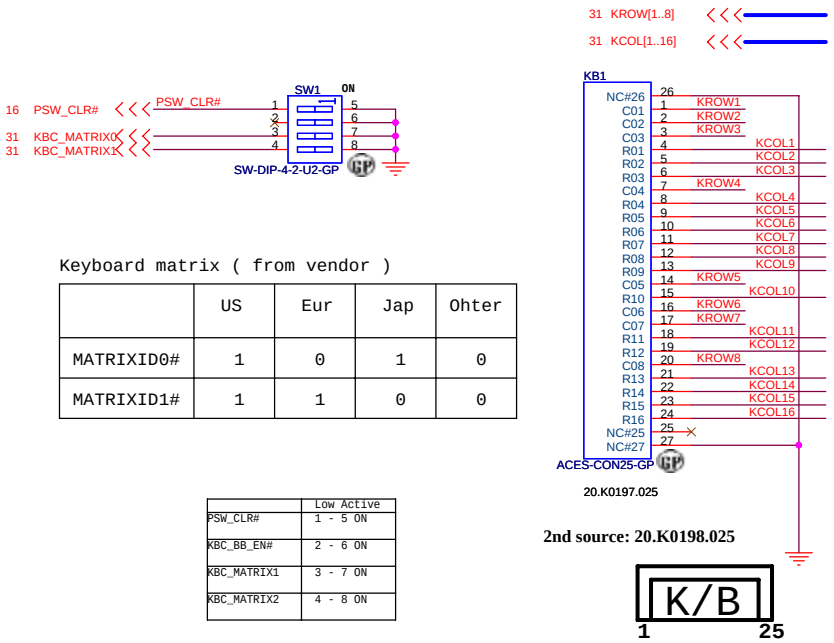
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SIO 87392 / FIR***

Size	Document Number	Rev
A3	AG1	-1

Date: Wednesday, January 18, 2006 Sheet 32 of 45

Internal KeyBoard Connector

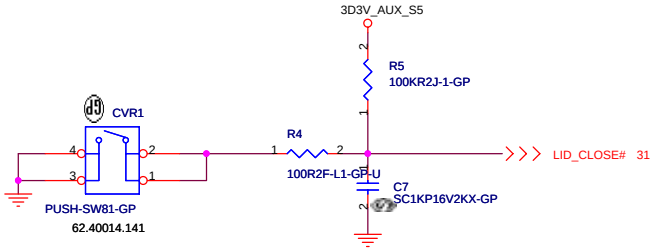


Keyboard matrix (from vendor)

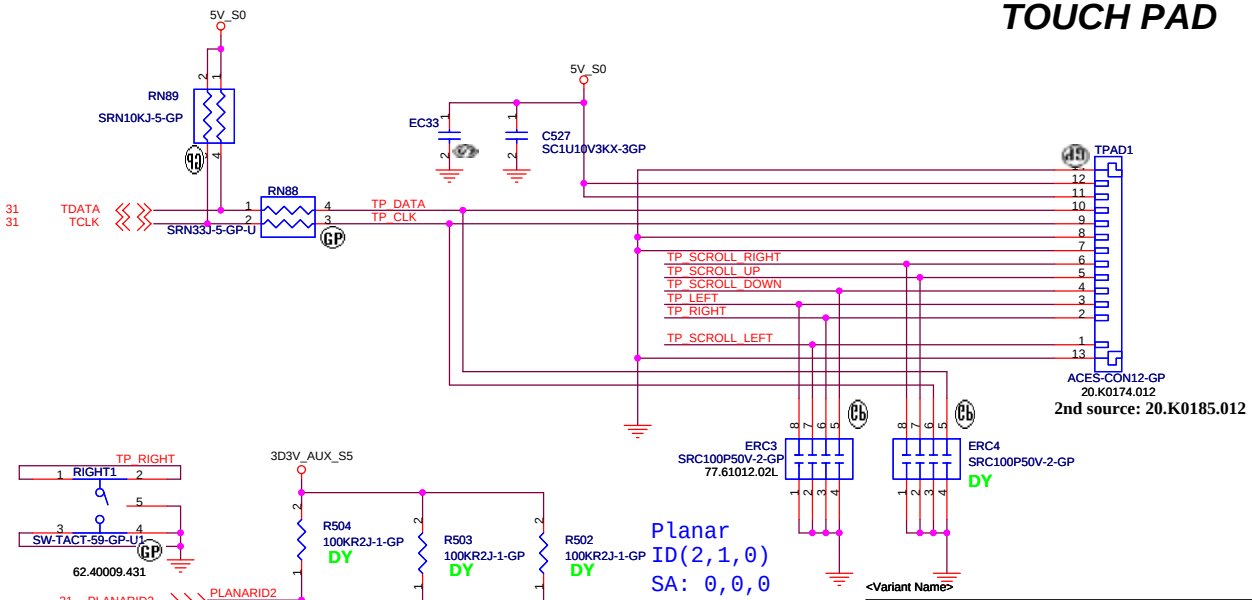
	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0

	Low Active
PSW_CLR#	1 - 5 ON
KBC_BB_EN#	2 - 6 ON
KBC_MATRIX1	3 - 7 ON
KBC_MATRIX2	4 - 8 ON

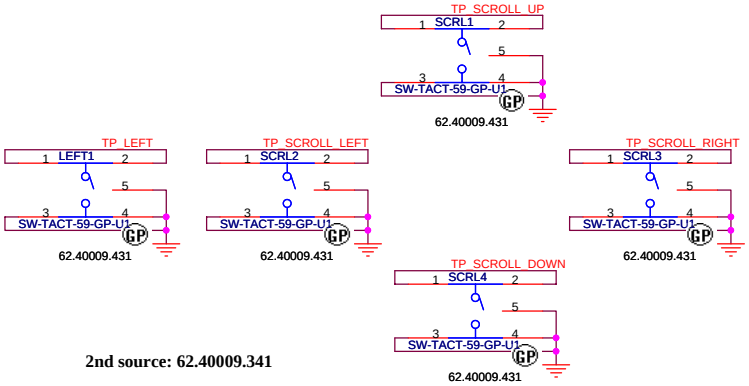
COVER SWITCH

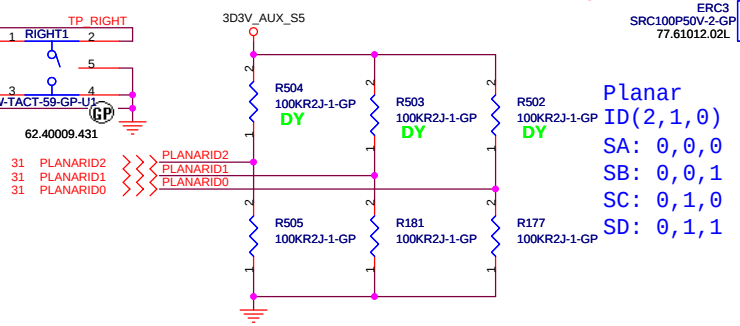


TOUCH PAD



SCROLL KEY

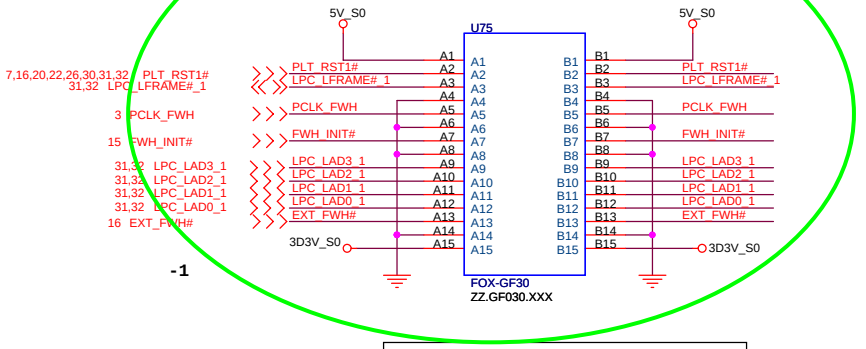




<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	KEYBOARD/TOUCHPAD	
Size A3	Document Number AG1	Rev -1
Date: Wednesday, January 18, 2006	Sheet 33 of 45	

GOLDEN FINGER FOR DEBUG BOARD

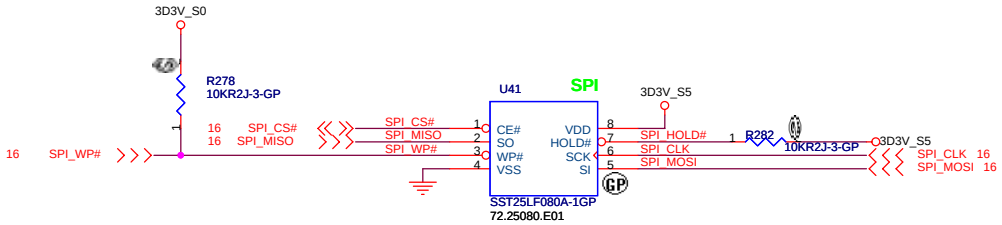


-1

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

SPI FLASH ROM

8M Bits



SOIC 200 Socket P/N:
Wieson: 62.10076.001
SPI ROM:
SST25LF080A: 72.25080.E01
SST25VF080B : 72.25080.G01
ST M25P80: 72.25P80.001

TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

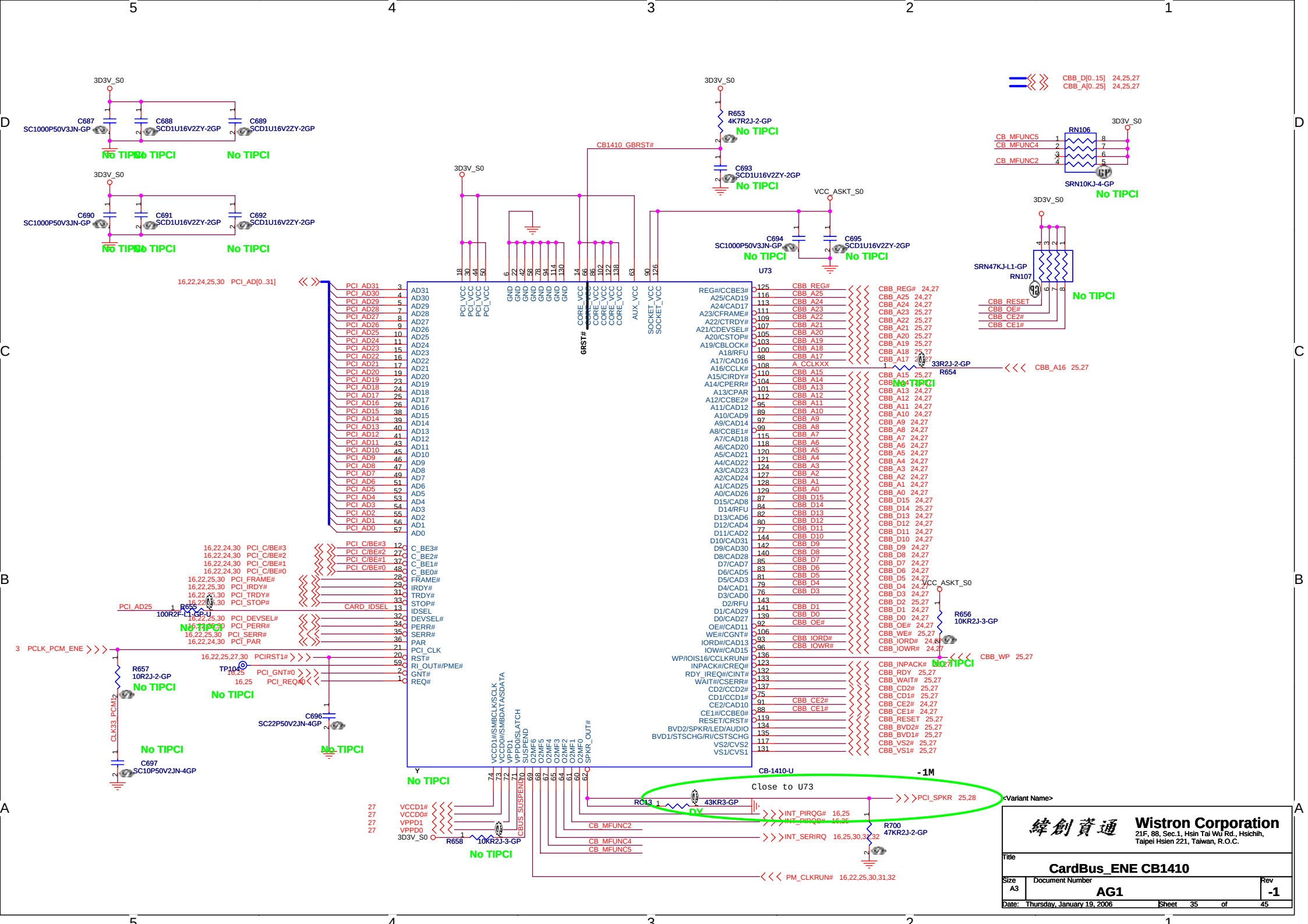
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

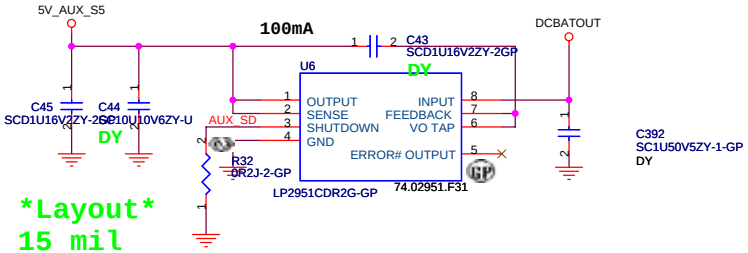
Title: ***BIOS : SPI***

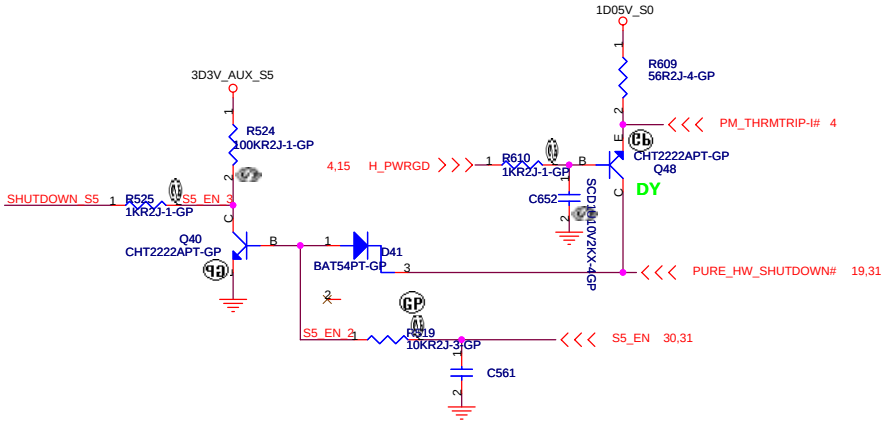
Size	Document Number	Rev
A3	AG1	-1

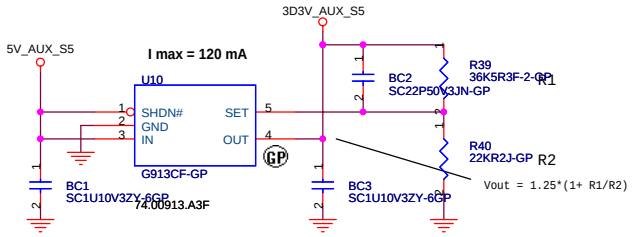
Date: Wednesday, January 18, 2006 Sheet 34 of 45

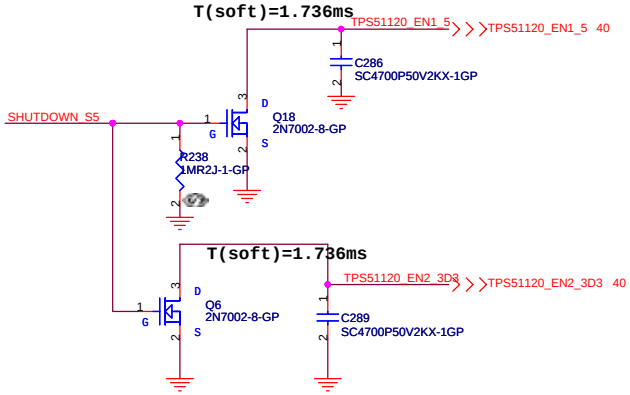

3D3V_S0
C687 SC1000P50V3JN-GP
C688 SCD1U16V2ZY-2GP
C689 SCD1U16V2ZY-2GP
C690 SC1000P50V3JN-GP
C691 SCD1U16V2ZY-2GP
C692 SCD1U16V2ZY-2GP
No TIPCI
R653 4K7R2J-2-GP
C693 SCD1U16V2ZY-2GP
CB1410_GBRST#
VCC_ASKT_S0
C694 SC1000P50V3JN-GP
C695 SCD1U16V2ZY-2GP
CBB_D[0..15] 24,25,27
CBB_A[0..25] 24,25,27
RN106
CB_MFUNC5
CB_MFUNC4
CB_MFUNC2
SRN10KJ-4-GP
SRN47KJ-L1-GP
RN107
CBB_RESET
CBB_OE#
CBB_CE2#
CBB_CE1#
U73
16,22,24,25,30 PCI_AD[0..31]
PCI_AD31 PCI_AD30 PCI_AD29 PCI_AD28 PCI_AD27 PCI_AD26 PCI_AD25 PCI_AD24 PCI_AD23 PCI_AD22 PCI_AD21 PCI_AD20 PCI_AD19 PCI_AD18 PCI_AD17 PCI_AD16 PCI_AD15 PCI_AD14 PCI_AD13 PCI_AD12 PCI_AD11 PCI_AD10 PCI_AD9 PCI_AD8 PCI_AD7 PCI_AD6 PCI_AD5 PCI_AD4 PCI_AD3 PCI_AD2 PCI_AD1 PCI_AD0
AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
PCI_VCC PCI_VCC PCI_VCC PCI_VCC
GND GND GND GND GND GND GND GND
CORE_VCC CORE_VCC CORE_VCC CORE_VCC CORE_VCC CORE_VCC CORE_VCC
AUX_VCC
SOCKET_VCC SOCKET_VCC
GRST#
REG#/CCBE3# A25/CAD19 A24/CAD17 A23/CFRAME# A22/CTRDY# A21/CDEVSEL# A20/CSTOP# A19/CBLOCK# A18/RFU A17/CAD16 A16/CCLK# A15/CIRDY# A14/CPERR# A13/CPAR A12/CCBE2# A11/CAD12 A10/CAD9 A9/CAD14 A8/CCBE1# A7/CAD18 A6/CAD20 A5/CAD21 A4/CAD22 A3/CAD23 A2/CAD24 A1/CAD25 A0/CAD26 D15/CAD8 D14/RFU D13/CAD6 D12/CAD4 D11/CAD2 D10/CAD31 D9/CAD30 D8/CAD28 D7/CAD7 D6/CAD5 D5/CAD3 D4/CAD1 D3/CAD0 D2/RFU D1/CAD29 D0/CAD27 OE#/CAD11 WE#/CGNT# IORD#/CAD13 IOW#/CAD15 WP/IOIS16/CCLKRUN# INPACK#/CREQ# RDY_IREQ#/CINT# WAIT#/CSERR# CD2/CCD2# CD1/CCD1# CE2/CAD10 CE1#/CCBE0# RESET/CRST# BVD2/SPKR/LED/AUDIO BVD1/STSCHG/RI/CSTSCHG VS2/CVS2 VS1/CVS1
CBB_REG# CBB_A25 CBB_A24 CBB_A23 CBB_A22 CBB_A21 CBB_A20 CBB_A19 CBB_A18 CBB_A17 A_CCLKXX CBB_A15 CBB_A14 CBB_A13 CBB_A12 CBB_A11 CBB_A10 CBB_A9 CBB_A8 CBB_A7 CBB_A6 CBB_A5 CBB_A4 CBB_A3 CBB_A2 CBB_A1 CBB_A0 CBB_D15 CBB_D14 CBB_D13 CBB_D12 CBB_D11 CBB_D10 CBB_D9 CBB_D8 CBB_D7 CBB_D6 CBB_D5 CBB_D4 CBB_D3 CBB_D1 CBB_D0 CBB_OE# CBB_IORD# CBB_IOWR# CBB_INPACK# CBB_RDY CBB_WAIT# CBB_CD2# CBB_CD1# CBB_CE2# CBB_CE1# CBB_RESET CBB_BVD2# CBB_BVD1# CBB_VS2# CBB_VS1#
R654 33R2J-2-GP
CBB_A16 25,27
R656 10KR2J-3-GP
CBB_WP 25,27
16,22,24,30 PCI_C/BE#3 PCI_C/BE#2 PCI_C/BE#1 PCI_C/BE#0
C_BE3# C_BE2# C_BE1# C_BE0#
16,22,25,30 PCI_FRAME# PCI_IRDY# PCI_TRDY# PCI_STOP#
FRAME# IRDY# TRDY# STOP#
PCI_AD25 R655 100R2F-L1-GP-U
CARD_IDSEL
16,22,25,30 PCI_DEVSEL# PCI_PERR# PCI_SERR# 16,22,24,30 PCI_PAR
IDSEL DEVSEL# PERR# SERR# PAR
3 PCLK_PCM_ENE
R657 10R2J-2-GP
CLK33_PCM12
16,22,25,27,30 PCIRST1#
TP104
16,25 PCI_GNT#0
16,25 PCI_REQ#0
PCI_CLK RST# RI_OUT#/PME# GNT# REQ#
C696 SC22P50V2JN-4GP
C697 SC10P50V2JN-4GP
VCCD1#/SMBCLK/SCLK VCCD0#/SMBDAT/SDATA VPPD1 VPPD0/SLATCH SUSPEND O2MF6 O2MF5 O2MF4 O2MF3 O2MF2 O2MF1 O2MF0 SPKR_OUT#
CB-1410-U
-1M
Close to U73
RC13 43KR3-GP
PCI_SPKR 25,28
INT_PIRQG# 16,25
INT_PIRQF# 16,25
INT_SERIRQ 16,25,30,31,32
R700 47KR2J-2-GP
27 VCCD1# 27 VCCD0# 27 VPPD1 27 VPPD0
R658 10KR2J-3-GP
CBUS_SUSPEND
CB_MFUNC2
CB_MFUNC4
CB_MFUNC5
PM_CLKRUN# 16,22,25,30,31,32
<Variant Name>
No TIPCI
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CardBus_ENE CB1410
Size A3
Document Number AG1
Rev -1
Date: Thursday, January 19, 2006
Sheet 35 of 45

Aux Power

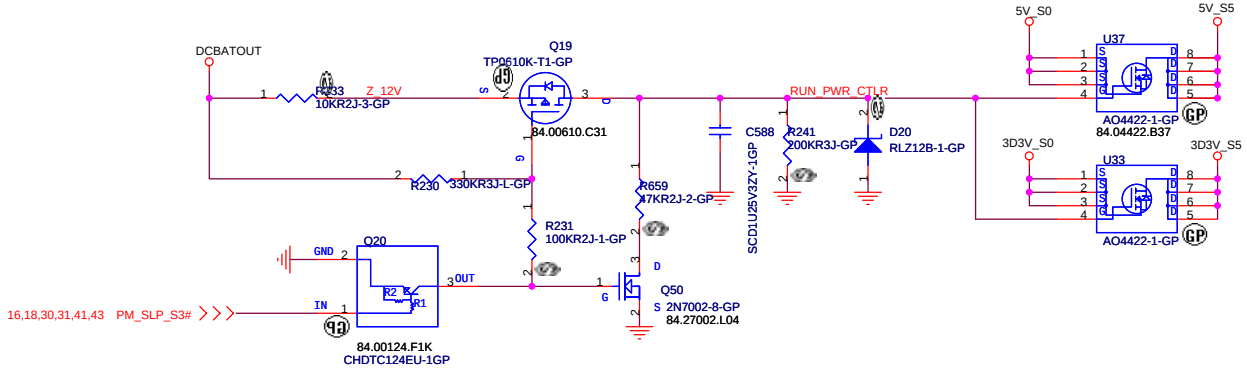








Run Power



<Variant Name>

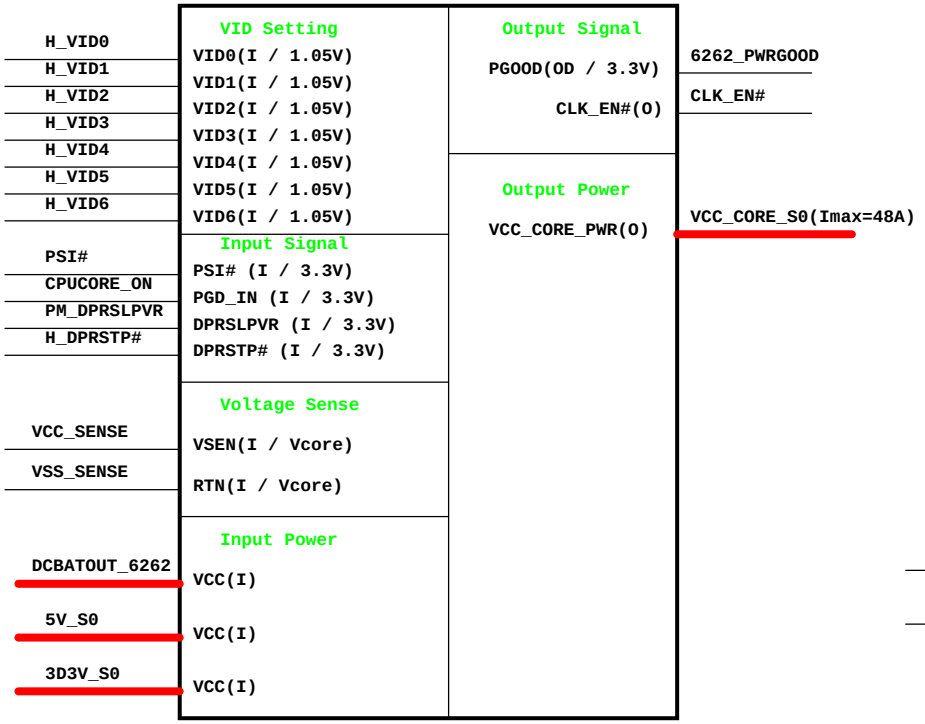
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN and AUX POWER**

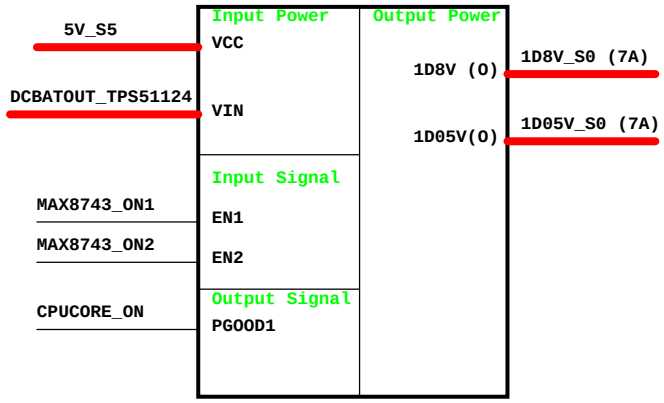
Size	Document Number	Rev
A3	AG1	-1

Date: Wednesday, January 18, 2006 Sheet 36 of 45

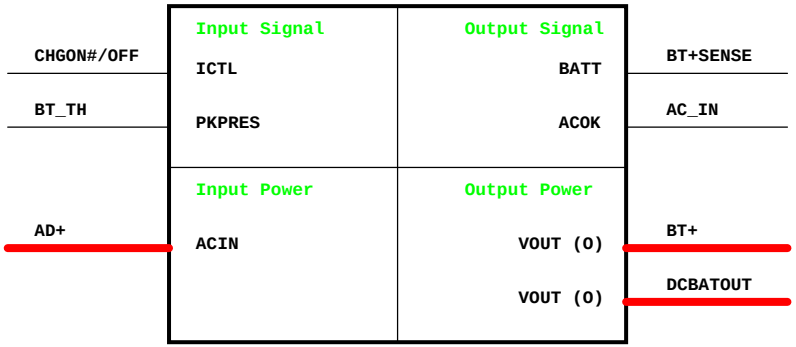
CPU_CORE
Intersil ISL6262



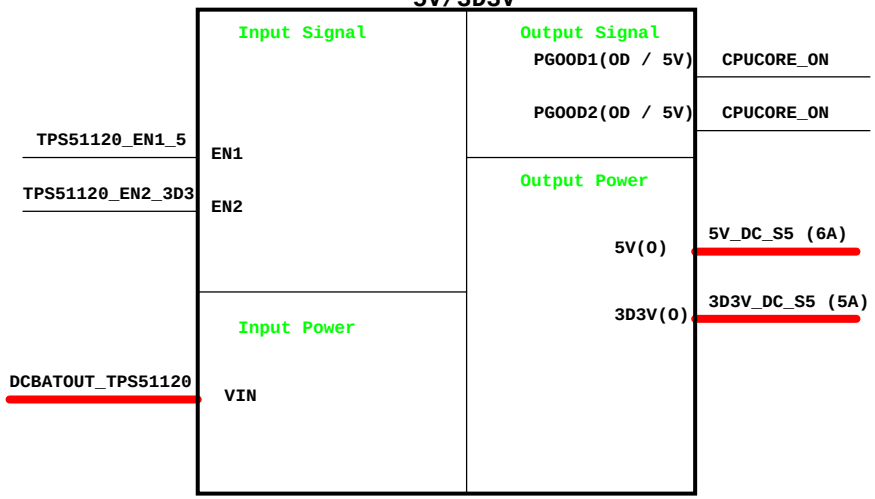
MAX8743
1D8V/1D05V



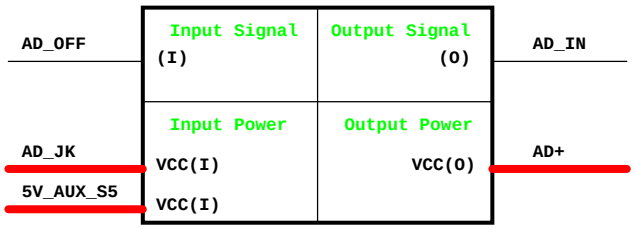
Charger Max8725



TPS51120
5V/3D3V



Adapter



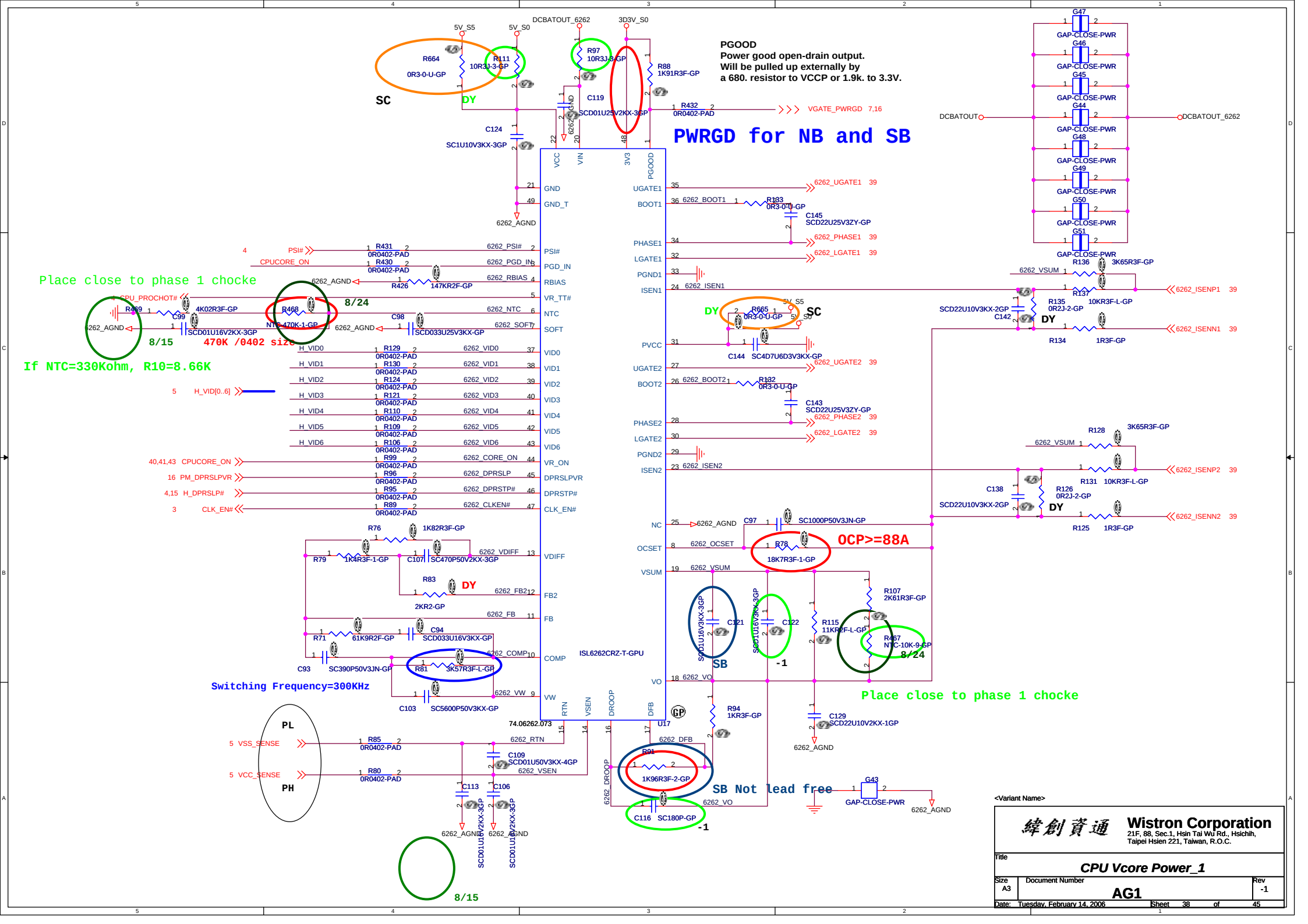
<Variant Name>

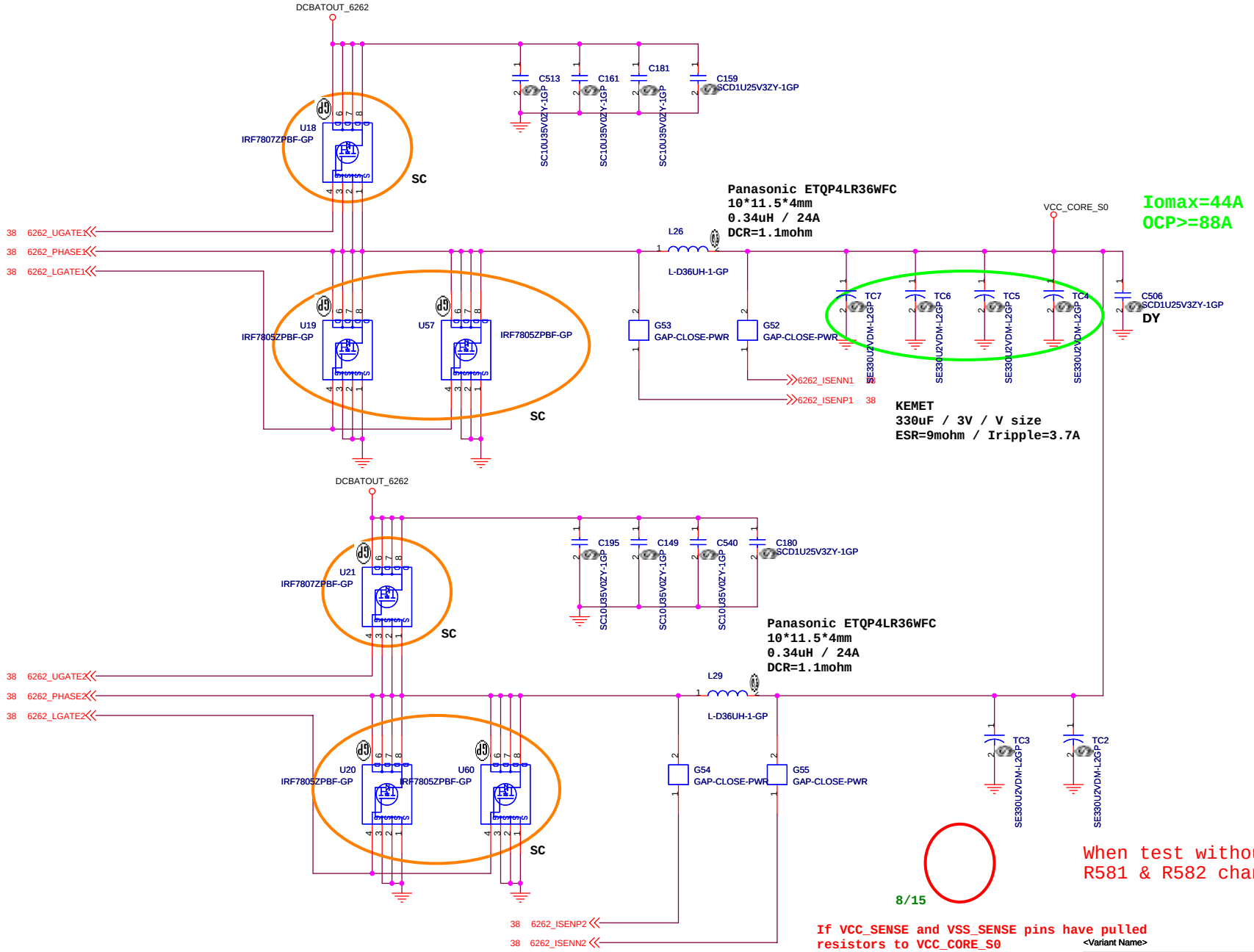
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

Size	Document Number	Rev
A3	AG1	-1

Date: Monday, January 09, 2006 Sheet 37 of 45

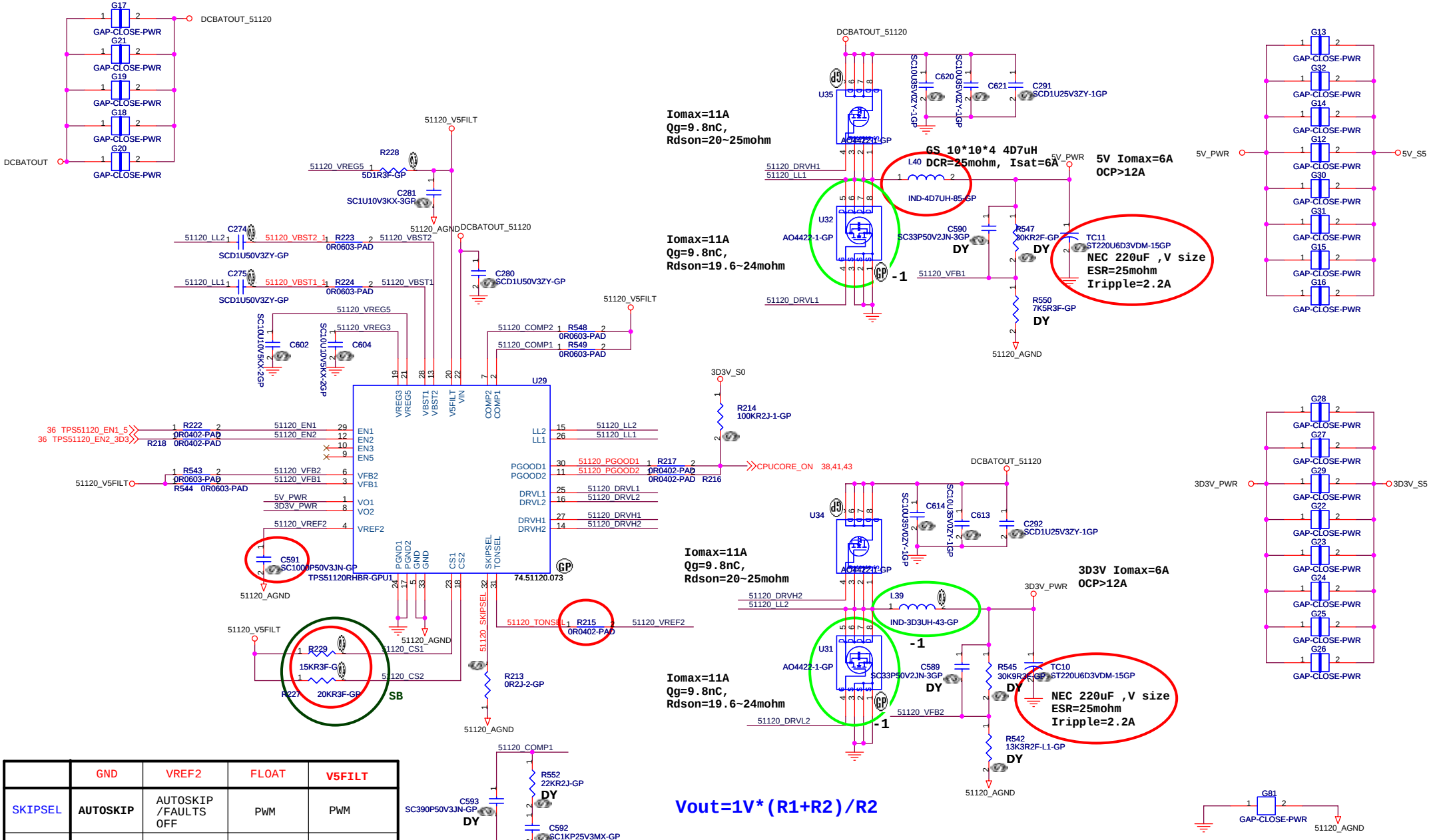

PGOOD
Power good open-drain output.
Will be pulled up externally by
a 680. resistor to VCCP or 1.9k. to 3.3V.
PWRGD for NB and SB
SC
DY
SB
PL
PH
ISL6262CRZ-T-GPU
Place close to phase 1 chocke
If NTC=330Kohm, R10=8.66K
470K /0402 size
8/24
8/15
Switching Frequency=300KHz
OCP>=88A
SB Not lead free
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore Power_1
AG1
Tuesday, February 14, 2006



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***CPU Vcore Power_2***	
Size: A3	Document Number: **AG1**	Rev: -1
Date: Wednesday, January 18, 2006	Sheet 39 of 45	



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	**Swithchr ON**	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

<Variant Name>

緯創資通 **Wistron Corporation**
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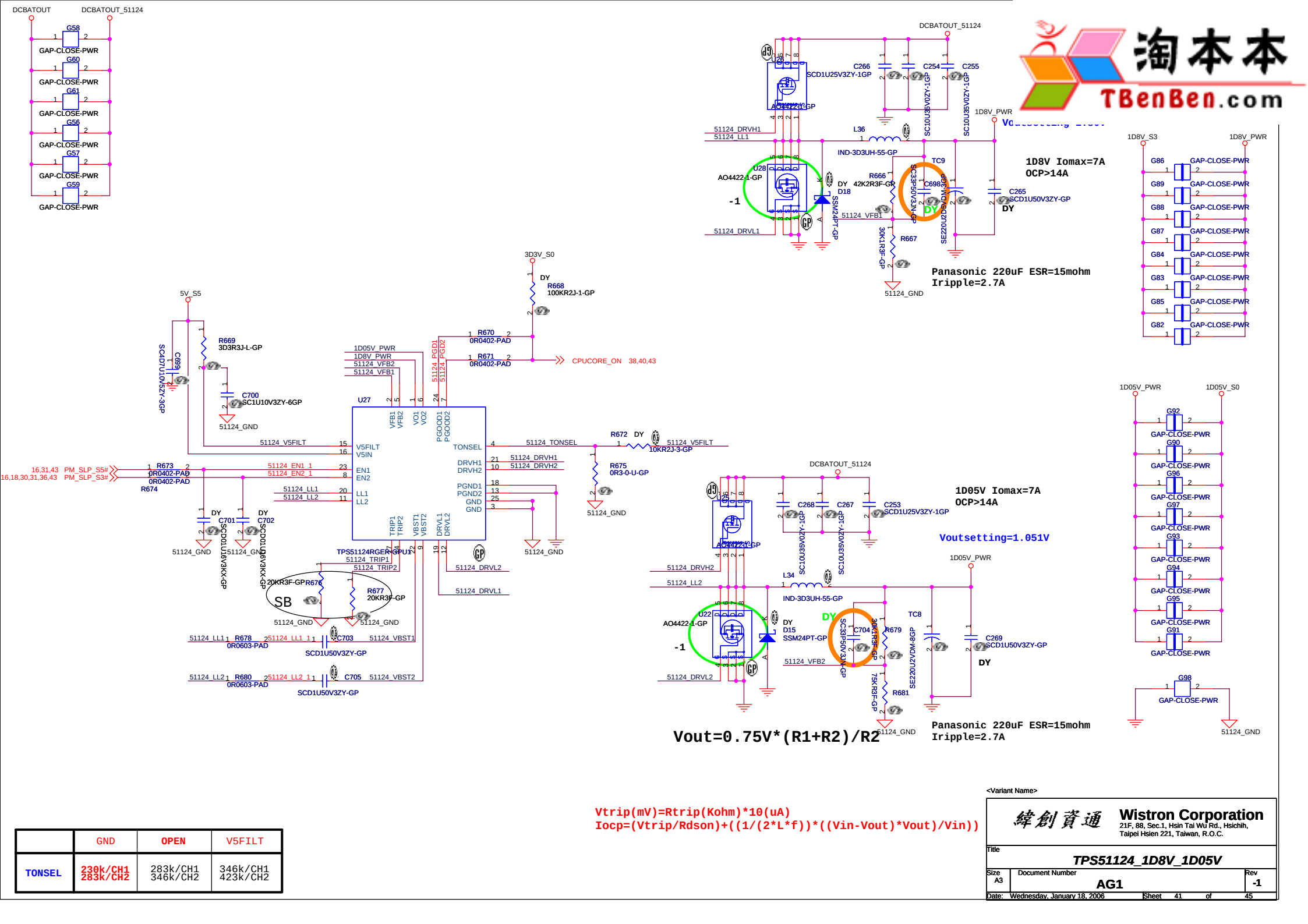
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***5V_UP_S5/3D3V_S5/5V_S5***

Size	Document Number	Rev
A3	**AG1**	-1

Date: Wednesday, January 18, 2006 Sheet 40 of 45



	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

<Variant Name>

Wistron Corporation
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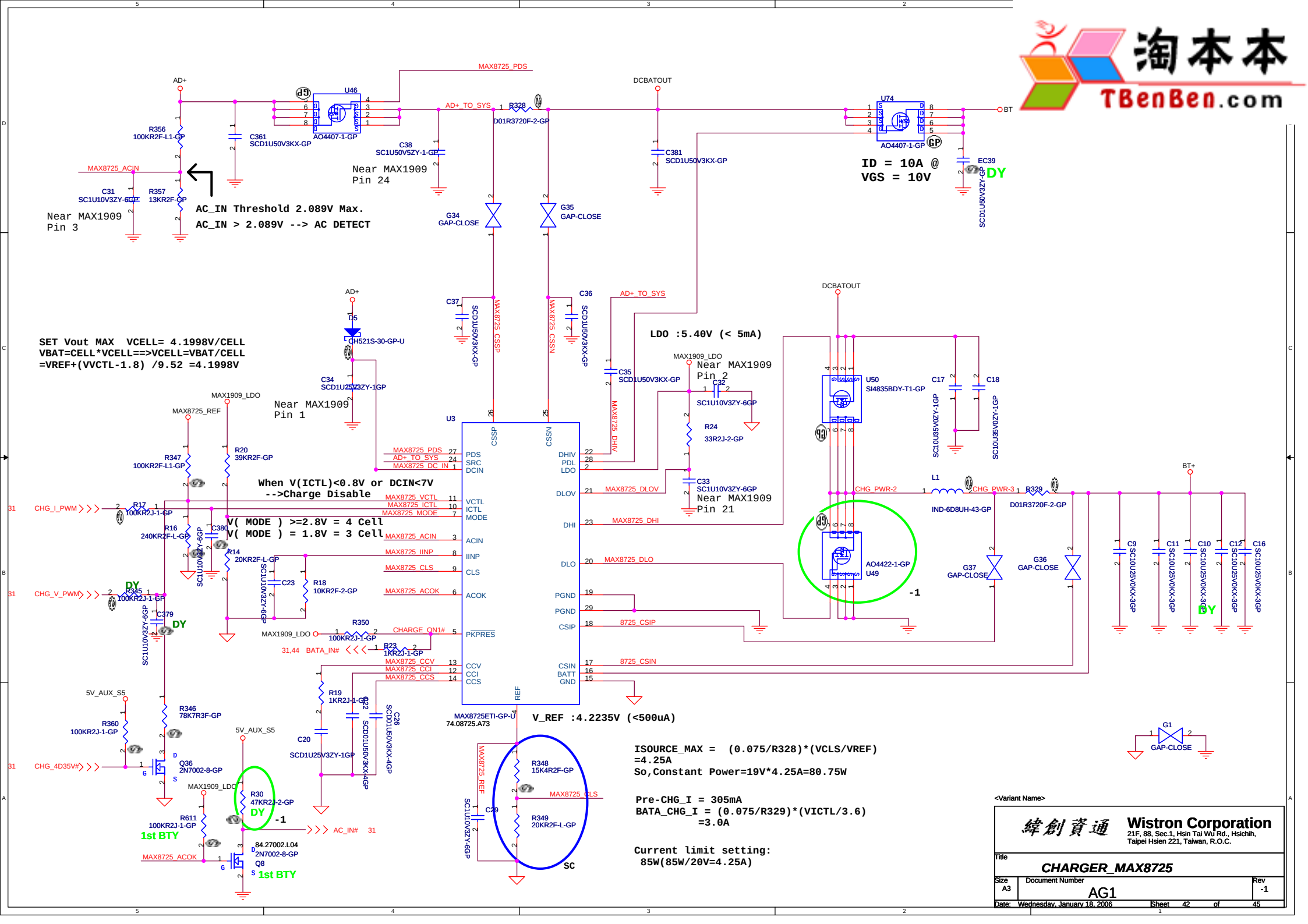
Taipei Hsien 221, Taiwan, R.O.C.

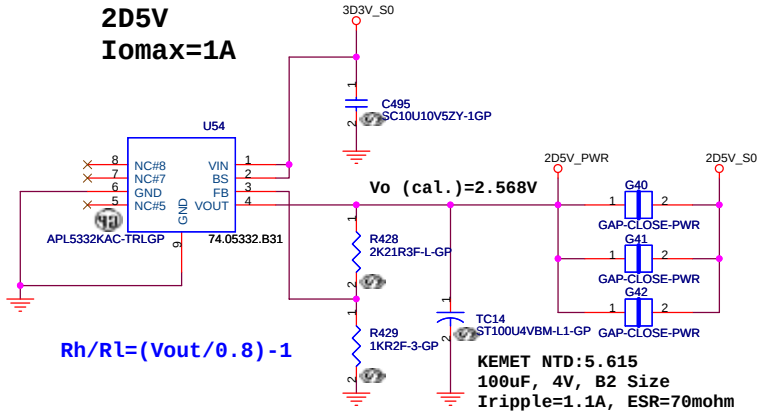
Title: TPS51124_1D8V_1D05V

Size	Document Number	Rev
A3	AG1	-1

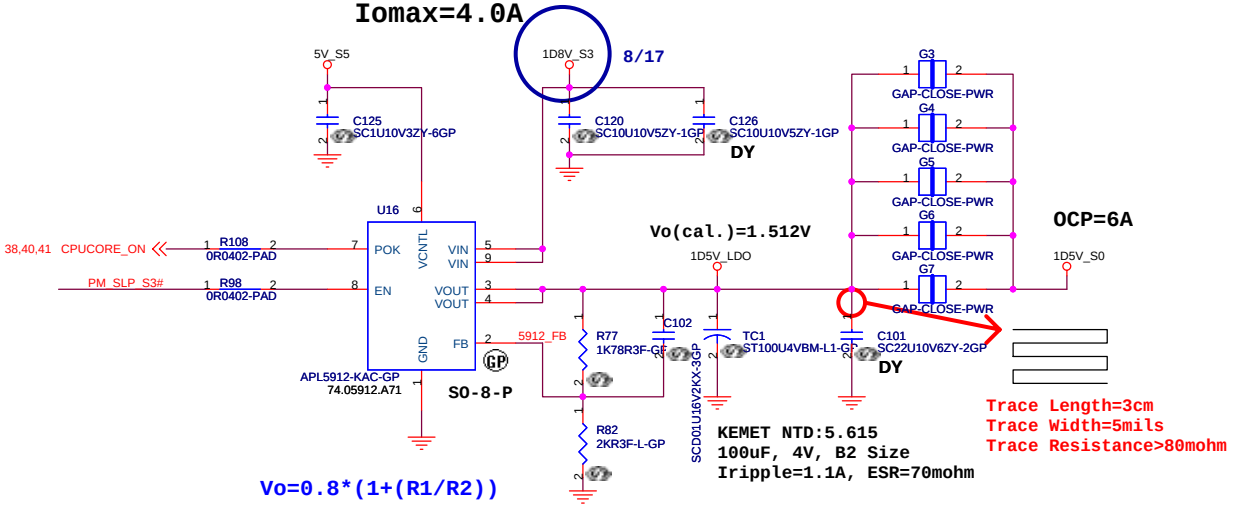
Date: Wednesday, January 18, 2006 Sheet 41 of 45



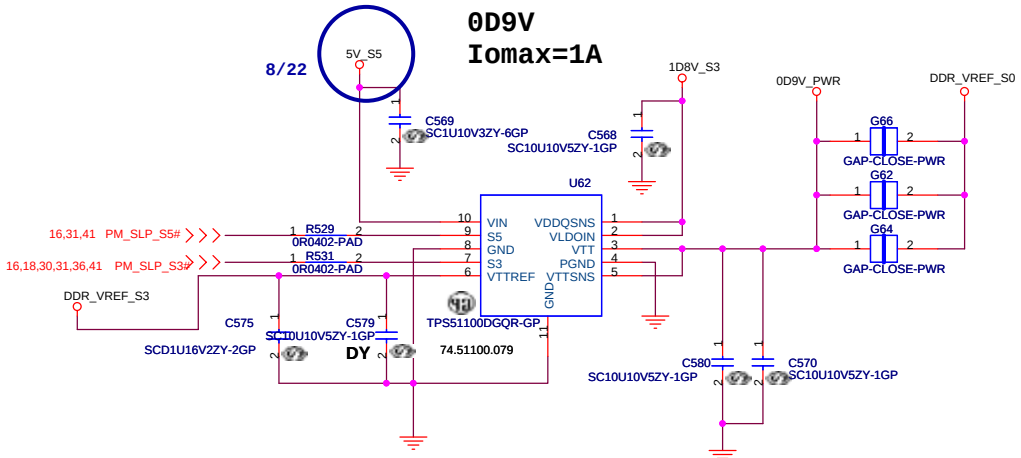
2D5V
Iomax=1A



1D5V_S0
Iomax=4.0A



0D9V
Iomax=1A



2nd source: 74.02997.079
G2997F6U

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	0D9V/1D5V/2D5V	
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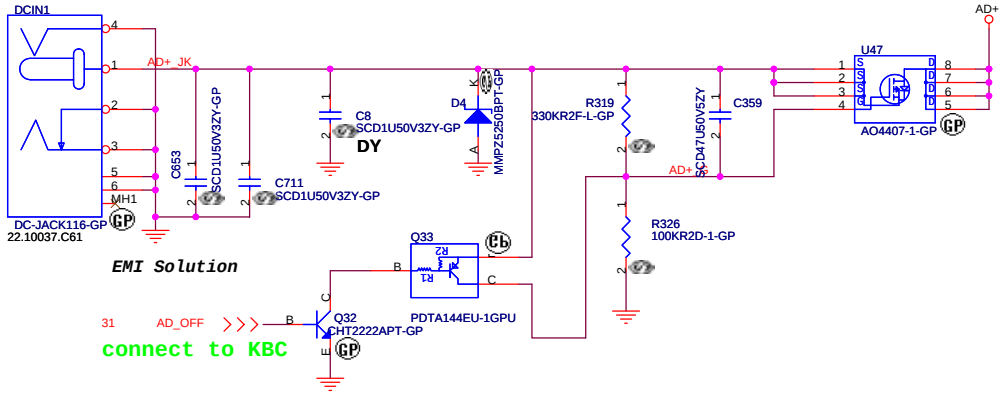
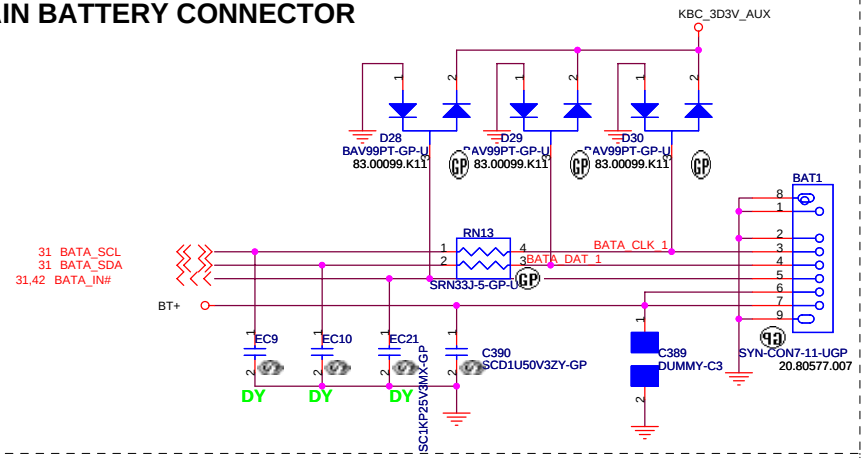
Date: Wednesday, January 18, 2006	Sheet 43 of 45	

ADAPTER IN CIRCUIT



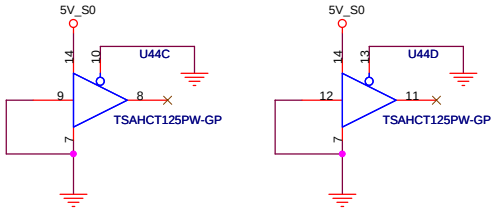
MAIN BATTERY CONNECTOR

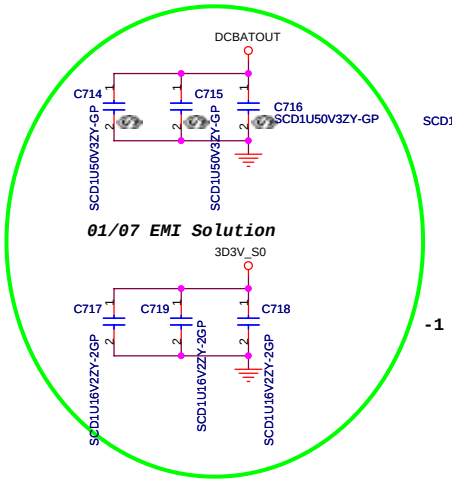


<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
Size A3	Document Number AG1	Rev -1
Date: Wednesday, January 18, 2006	Sheet 44 of 45	





SCD1U5

SCD1

SCD1

TOP SIDE:

New Card

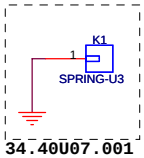
H17 HOLE

34.4A901.001

CPU Thermal Module

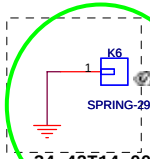
H29 HOLE H32 HOLE H31 HOLE

34.4A908.001



34.40U07.001

No New



34.42T14.001

-1

BOTTOM SIDE:

IO Bracket FOR MDC

H21 H22 H25 H27

34.4A902.001

IO Bracket

H30

34.4A903.001

IO Bracket

H34

34.4A904.001

H11

34.4A905.001

UMA

H7

34.4A906.001

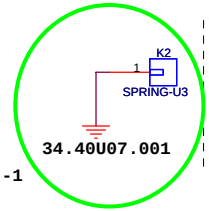
FOR MINIC

H28 H26

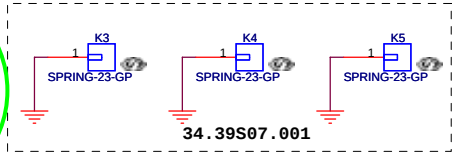
MINIC

MINIC 34.4A907.001

-1



34.40U07.001



34.39S07.001

H12 HOLE H15 HOLE H19 HOLE H2 HOLE H3 HOLE H35 HOLE H4 HOLE H10 HOLE H13 HOLE H8 HOLE H5 HOLE H18 HOLE H14 HOLE

H16 HOLE H1 HOLE H6 HOLE H9 HOLE H33 HOLE H20 HOLE

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SPRING & BOSS***

Size	Document Number	Rev
A3	AG1	-1

Date: Tuesday, January 24, 2006 Sheet 45 of 45